K-Bus Transceiver E910.05

PRODUCTION DATA - JUL 27, 2011

Features

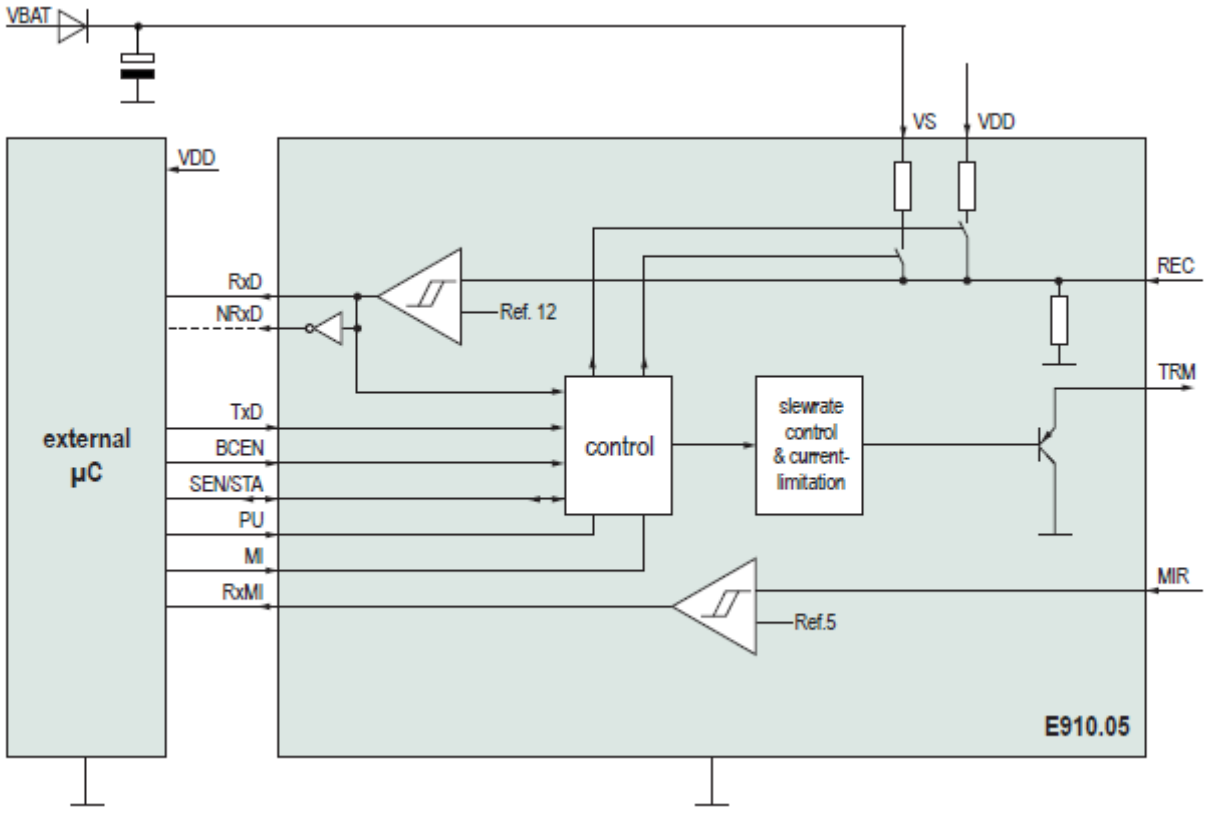
- K-Bus Interface useable as diagnostic interface to ISO 9141
- Data rate up to 9.600 Baud
- Very low standby current (30µA typical)
- Output slewrate control to reduce EMI
- Internal monitoring of prohibited conditions
- Supply voltage range VS 6.9V to 19V
- Supply voltage range VDD 4.5V to 5.5V
- Bus-line input voltage range – 24V to + 30V
- – 40°C to + 125°C operating temperature
- SO14n package

Applications

- Automotive bus systems

Brief Functional Description

The IC is designed for communication via bidirectional serial data channels. In addition to the level conversion of transmit and receive signals from the microcontroller's voltage level to the 12V bus level, the device includes plausibility checks in order to guarantee undisturbed bus communication in case of corrupted data from the microcontroller. Undefined states are avoided during low voltage conditions by means of a Power-on-Reset which blocks the outputs. The inputs feature internal pull-up and pull-down current sources to maintain defined levels. The bus pins TRM and REC feature a wide input voltage range from – 24V up to +40V.



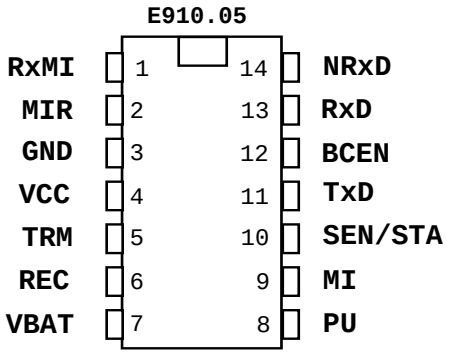
Typical Application

1. Package and Pinout

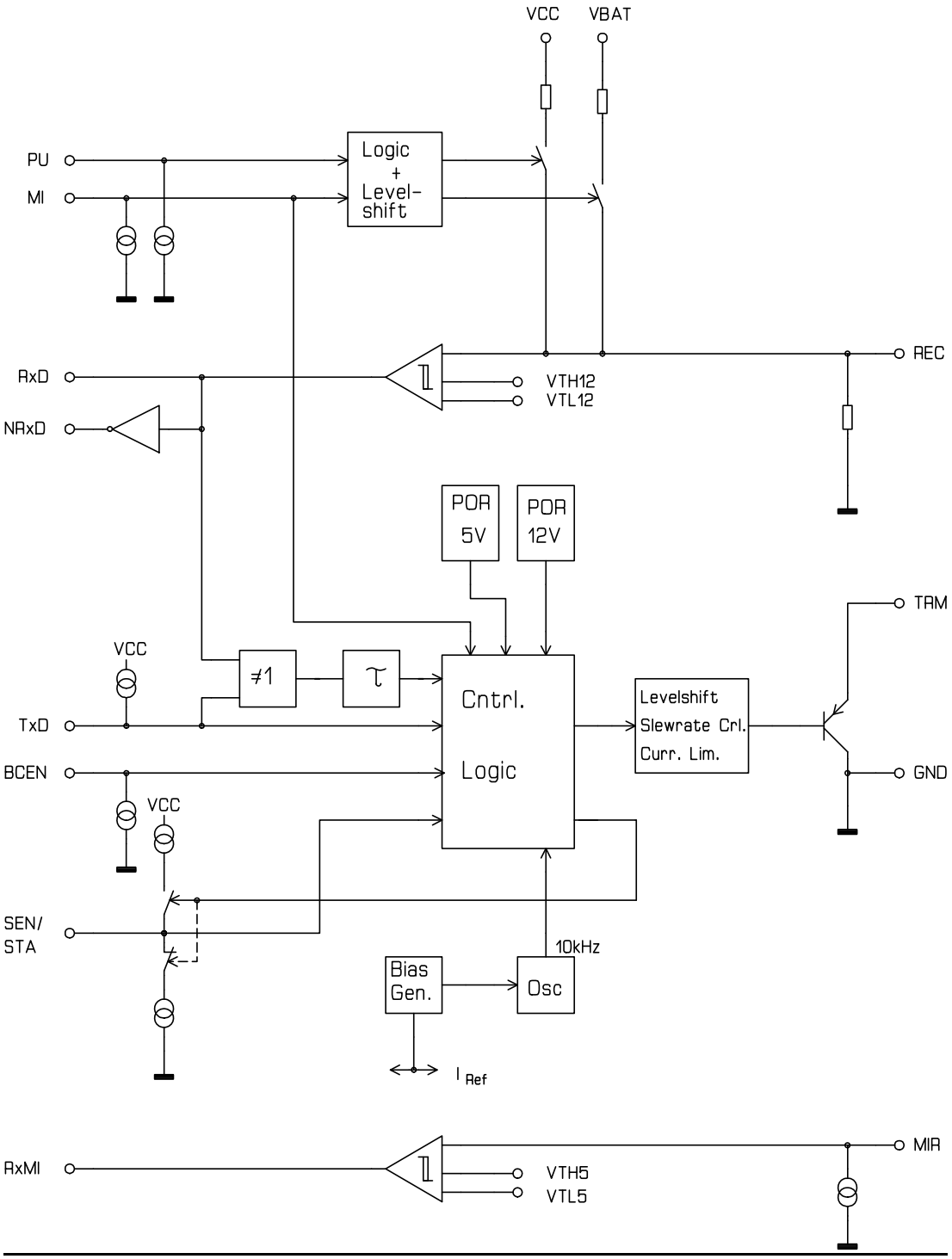
1.1. Package Pin Description

Pin	Name	Description
1	RxMI	Receive MI Bus, Output to MPU
2	MIR	MI Bus receive
3	GND	Ground
4	VCC	+5V Supply line
5	TRM	Transmit pin
6	REC	Receive pin
7	VBAT	+12V Battery supply
8	PU	Activate pull-up
9	MI	MI Bus enable
10	SEN/STA	Transmit path status
11	TxD	Transmit data, input from MPU
12	BCEN	Enable Bit Compare Function
13	RxD	Receive data, output from MPU
14	NRxd	Inverted receive data

1.2. Package Pin Out



2. Block Diagram



3. Operating Conditions

3.1. Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
All voltages referred to ground (GND). Currents flowing into terminals are signed as positive, those drawn out of a terminal are negative.

Parameter	Pin	Symbol	min	max	Unit
Supply voltage	4	V_{CC}	- 0.3	6.5	V
Supply current	4	I_{CC}		10 0	mA
Battery voltage for T<500ms	7	V_{BAT}	- 0.3	30 0 40 0	V V
Supply current	7	I_{BAT}		20 0	mA
Input voltage	8-12	V_{IN}	- 0.3	V_{CC} + 0.3	V
Input current	8-12	I_{IN}	- 10.0	10 0	mA
Input voltage	2	V_{IN}	- 0.3	V_{BAT}+0.3	V
Input current	2	I_{IN}	- 10.0	10 0	mA
Input voltage for T<500ms	5,6	V_{IN}	- 24.0	30 0 40 0	V V
Output current	13,14	I_{OUT}	- 10.0	10 0	mA
Power dissipation TA = 85 °C		P_{TOT}		420 0	mW
Thermal Resistance (Junction to Ambient)		Rth_{J-A}		165 0	K/W
Junction Temperature		T_J		+ 150 0	°C
Operating Range		T_{OPT}	- 40.0	+ 125 0	°C
Storage Temperature		T_{STG}	- 55.0	+ 150 0	°C

3.2. Recommended Operating Conditions

The following conditions apply unless otherwise stated.

Parameter	Pin	Condition	Symbol	min	typ	max	unit
Power On Res. Level V_{CC}	4		V_{CCPOR}	2.8	3.5	4.2	V
Power On Res. Level V_{BAT}	7		V_{BATPOR}	3.0	3.8	4.5	V
Supply Current $I_{CC}+I_{BAT}$	3	V_{CC} = 5,0V, V_{BAT} = 12,0V Pins 1, 2, 5, 6, 8..14 open	I_{CCBAT}		30.0	50.0	µA
Pull down Current PU, MI, BCEN	8, 9, 12		I_{pd}	160.0	250.0	330.0	µA
Pull up Current TxD	11		I_{pu}	-330.0	-250.0	-160.0	µA
Pull down Current SEN/STA	10		I_{pdSen}	160	250	330.0	µA
Pull up Current SEN/STA	10		I_{puSen}	-330.0	-250.0	-160.0	µA
Input Low Level PU,MI,BCEN,TxD,SEN/STA	8, 9, 10, 11, 12		V_{IL}			0.25	V_{CC}
Input -High Level PU,MI,BCEn,TxD,Sen/Sta	8, 9, 10, 11, 12		V_{IH}	0.75			V_{CC}
Pull down Current MIR	2		I_{pd}	27.0	43.0	60.0	µA
Input Low Level MIR	2		V_{IL}			1.4	V
Input High Level MIR	2		V_{IH}	2.5			V
Input Low Level REC	6		VIL			0.4	VBAT
Input High Level REC	6		V_{IH}	0.6			VBAT
Hysteresis,	6		V_{Hys}		50.0		mV
Input Resistance REC without Pull up	6	Tamb < 85°c	R_{IN} R_{IN}	330.0	800.0	1500.0 1300.0	kΩ kΩ
5 Volt Pull up Resistance REC	6	V_{CC} = 5V, V_{out} Pin 6 = 0V	R_{pu5}	1.4	2.2	3.0	kΩ
12 Volt Pull up Resistance REC	6	V_{BAT} = 12V V_{out} Pin 6 = 0V	R_{pu12}	1.4	2.2	3.0	kΩ
Maximum Active Output Voltage REC	6	V_{BAT} = 30V	$V_{0\ max}$	18.0	24.0		V
Output Voltage TRM under load	5	V_{CC} = 5,0V, V_{BAT} = 12,0V Pin 10 = 0V A) Pin 5: Load Current = 40mA B) Pin 5: Load Current = 10mA	 V_{out} V_{out}		 1.1 0.8	 1.4 1.0	 V V

Parameter	Pin	Condition	Symbol	min	typ	max	unit
Output Sink Current TRM (Current Limit)	5	V_{OUT} > Vfb	I_{lim}	30.0	70.0	140.0	mA
Output Sink Current TRM (before Fold Back)	5		I_{out}			180.0	mA
Fold Back Onset Voltage	5		V_{fb}			3.5	V
Input Resistance TRM	5	V_{out} = -23 V V_{out} = -12 V	R_{in}	15.0 40.0	40.0 80.0		kΩ kΩ
Output Leakage TRM	5	V_{OUT} = 16V	ILeak			5.0	µA
Output Voltage RxD, RxMI	1, 13	I_O = 1mA	V_{OL}			0.2	VCC
Output Voltage RxD, RxMI	1, 13	I_O = -1mA	V_{OH}	0.8			VCC
Output Voltage NRxD	14	I_O = 1mA	V_{OL}			0.2	VCC
Output Voltage NRxD	14	I_O = -1mA	V_{OH}	0.8			VCC

3.1.2 A.C. Characteristics

Parameter	Pin	Condition	Symbol	min	typ	max	unit
Slew Rate Control TRM in KIP Mode	5		dV/dT fall dV/dT rise	-2.5 1.0	-1.5 1.5	-1.0 2.5	V/µs
Debounce Time REC	6, 13	T > 85°C high impulse low impulse	t_{debh} t_{debh} t_{debl}	1.5 1.5 2.5	2.8 2.8 4.8	5.5 5.0 7.0	µs µs µs
Delay Time TxD->RxD/NRxD	11, 13	KIP Mode	t_{del}			20.0	µs
Delay Time TxD->RxMI	1, 11	MI-Mode	t_{del}	0.5		4.0	µs
Bit Compare Time	6, 10, 11		t_{bc}	35.0	40.0	70.0	µs
Recovery Time	5, 6, 11		t_{recov}	30.0	50.0	75.0	µs
Delay Time for Transmit Branch	5, 6, 11		t_{sperr}	0.920	1.36	1.8	ms
Permanent Low switch-off Time	5, 6, 11		t_{low}	3.0	6.0	12.0	ms
Oscillator Frequency	10		f_{osc}	8.0	12.0	15.0	kHz

4. Functional Description

4.1. General

The 910.05 Bus Interface is designed for the control of serial data channels. In addition to the level translation of Transmit and Receive signals from the processor voltage levels to the 12V bus levels, the device includes watchdog functions to ensure continued bus communication in the event of a failure of an individual bus member.
Undefined states are avoided during low voltage conditions by means of a Power-on-Reset which connects and disconnects the outputs and inputs. The inputs make use of internal Pull-up and Pull-down-resistors to maintain defined levels.

The bus control pins TRM and REC can operate or maintain a high impedance state from voltages between -24V and 40V independent of V_{BAT} and V_{CC}. This ensures that an open circuit ground connection or power supply interruption does not inhibit the operation of other devices using the bus.

4.2. Transmitter Path

When the Transmitter path is free, a Low level on the TxD pin switches the open-collector transistor on the TRM Pin on. In order to minimise the EMC radiation on the bus the rise and fall time of the transmit pulse on the TRM pin is conditioned by a slew rate controller. (MI = "0").

4.3. Receiver Path

The signal on the REC pin is permanently available at RxD and inverted on the NRxD pin. Transients are filtered by an internal debounce circuit on the comparator input.

The PU and MI pins can be programmed by the connection of a pull-up resistor to the V_{CC} or V_{BAT} supply (See Table)

For MI bus use (MI = "1") the device provides a second receive path the MIR pin and the RxMI output pin. The accompanying comparator thresholds are independent of the supply voltages and have a negligible delay time.

4.4. Bit-Compare-Function

If the TXD and REC signals differ by more than T_{bc} the transmitter path is disabled. The transmit path is only made available again after TxD and REC are High for at least t_{sperr} and no new disable signal is generated by the Bit-Compare-Function.

The Bit-Compare-Function is activated when the SEN/STA pin is open and the Pins MI and BCEN are at "0"
(See Table).

4.5. Permanent-low-Disconnection

The presence of a Low level on the TxD-Pin for time t_{low} (SEN/STA open, MI="0"),disables the transmitter path. A High-level on TxD for at least t_{recov} during the duration of t_{low} resets the permanent Low timer.

A disabled transmit path is only made available again when TxD and REC are High for longer than t_{sperr} and no new disable is generated by the Bit-Compare-Function or the Permanent Low Disconnection.

4.6. SEN/STA

The bi-directional pin SEN/STA flags the Transmitter status in KIP-Mode (MI = 0). The transmit path is disabled when SEN/STA = "1" and enabled when SEN/STA = "0". Since the driver capability of this pin is low (typically. 250µA) this can be overwritten by the microprocessor, ("Forced transmit status").

4.7. Functional Tables

4.7.1. Pull-up-Resistor

PU	MI	Pull-up
0	0	disabled
0	1	to VCC (5V) MI-Mode
1	0	to VBAT (12V)
1	1	to VBAT MI-Mode

4.7.2. Bit Compare-Function

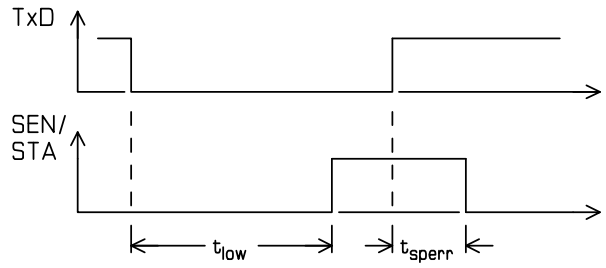
BCEN	MI	Bit Compare
0	0	active
1	0	inactive

4.7.3. Status Transmitter

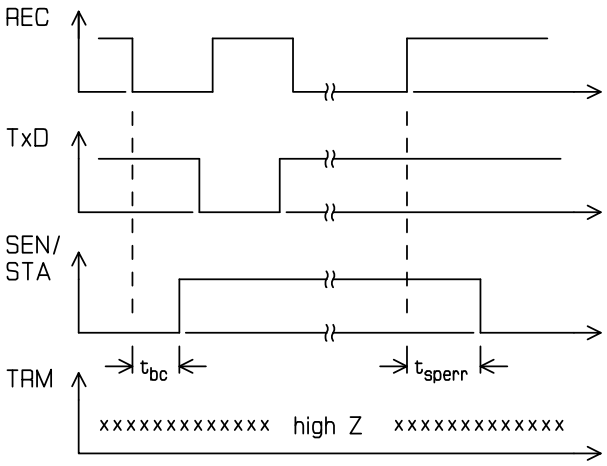
SEN/STA	MI	Transmitter
0	0	enabled
1	0	disabled
0	1	enabled
1	1	enabled

4.8. Timing Diagram

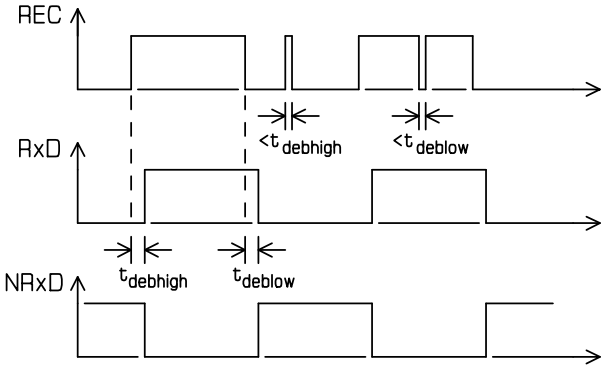
Permanent Low Shut Down



Bit Compare Function



Input Signal Debouncing

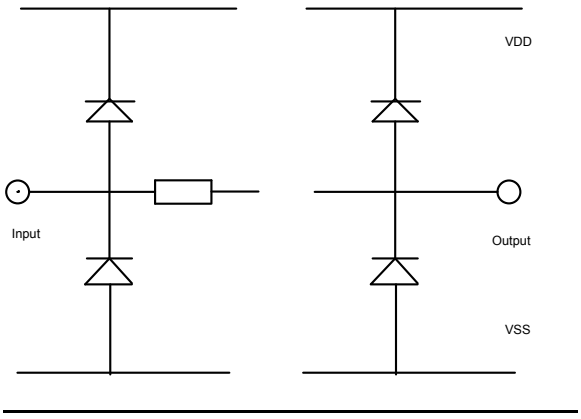


4.9. Noise Immunity

The 910.05 device meets the following requirements of DIN 40 839 part 1, when used in an application according to this specification :

Parameter	**Condition**	
Test pulse 1	t_1 = 5s / U_S = -100V	100 pulses
Test pulse 2	t_1 = 0,5s / U_S = 100V	1000 pulses
Test pulse 3a/b	DIN 40 839 Part 3 U_S = -150V / U_S = 100V	1000 Bursts
Test pulse 4	U_s =-6V U_a =-5V t_8 = 5s	10 pulses
Test pulse 5	R_i = 2_ t_D = 250ms t_r = 0,1ms U_P+U_S= 40V	10 pulses at 1 minute intervals

4.10. ESD Protection Circuit

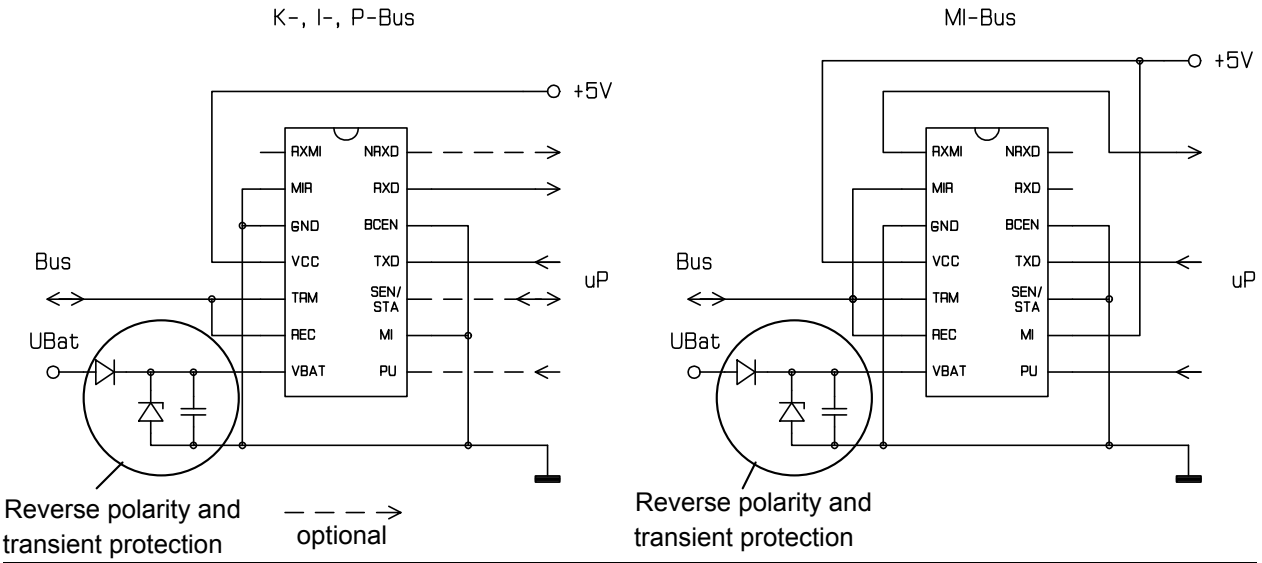


4.10.1. Test Method

The ESD Protection circuitry is measured using MIL-STD-883C Method 3015 (Human Body Model) with the following conditions :

VIN = 1000 Volt
REXT = 1500 Ohm
CEXT = 100 pF

4.11. Operating Circuit



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