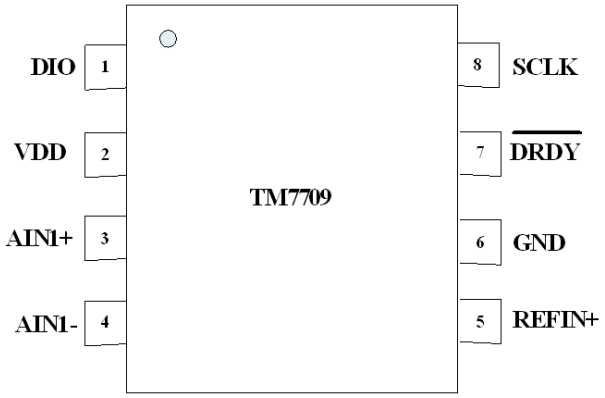
I Overview

The TM7709 is a single channel analog front end that is applied to low frequency measurement. The device can accept low level input signals directly from a transducer and then generate serial digital output. 24-bit no missing codes performance can be achieved by using Σ-Δ conversion technology. The selected input signal is sent to a special programmable gain front end based on an analog modulator. The output signal of the modulator is processed by an on-chip digital filter. The TM7709 operates from a single power supply (2.7~3.3V or 4.75~5.25V). It features a fully differential analog input as well as a differential reference input. The TM7709 is an ideal product used for intelligent, micro-controller and DSP-based systems. It features a serial interface that can be configured as second-wire interface. The internal structure of the chip can ensure that the device has very low power consumption and power-down mode to reduce power consumption while in standby.

II Features

- ADC input by fully differential single channel
- 24-bit no missing codes
- 0.003% nonlinearity
- Gains of 16/128 (optional)
- Second-line serial interface
- 2.7 ~ 3.3V or 4.75 ~ 5.25V operating voltage
- Package: SOP8

III Pin assignment and function



Pin	Name	Function
1	**DIO**	serial data inputs and outputs, with internal 10K pull-up resistors
2	**VDD**	Positive power supply voltage
3	**AIN1+**	Positive input end of differential analog input channel
4	**AIN1-**	Negative input end of differential analog input channel
5	**REFIN+**	Positive reference input end
6	**GND**	Ground
7	**$\overline{DRDY}$**	Logic output. A logic low on the output end indicates that a new output word is available from the TM7709 data register. The DRDY pin returns high upon completion of a read operation of a full output word. If no data read occurs between the two output updates, the DRDY will return high for 500 ×t_{CLKIN} prior to the next output update. While DRDY is high, a read operation should not be attempted or in progress to avoid reading from the data register as it is being updated. The DRDY returns low again when the data is updated.
8	**SCLK**	Serial clock (Schmitt logic input)

IV Serial Communication

(1) Command:

a) Write to setup Register command: BFH

b) Read access to DRDY command: 3FH

c) Once 3F command is issued, the chip will have a continuous output of DRDY information with 8 SCLK. When the DRDY being read is low, it indicates that the data have been converted and the data in the data register can be read.

d) Read access to the data register: 7FH

(2) Register table:

■ Setup register: 8 bits (the initial value is 0010_0000B)

7	6	5	4	3	2	1	0
$\overline{0/DRDY}$	CH	GAIN	STBY	0	0	0	0

CH: 0 means Channel 1 is connected;

GAIN: 0 means gain is set as 16; 1 means gain is set as 128.

STBY: 0 means normal operating mode; 1 means standby mode.

■ Data register: 24 bits (the initial value is 0000H)

The data register is a 24-bit read-only register that includes the most up-to-date conversion result from the TM7709.

(3) Communications sequence

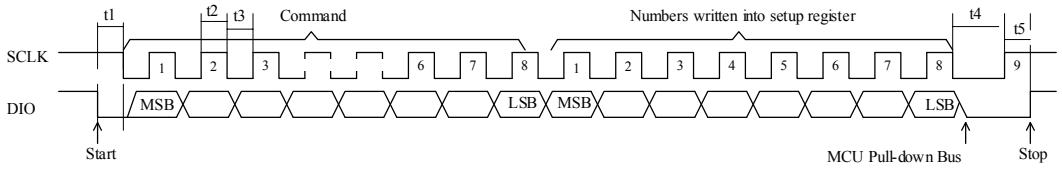
The chip adopts a similar IIC protocol to perform serial communication. The data in communication is sent from high bit to low bit. Any directive must start with the start flag and end with the stop flag. The chip accepts data on the rising edge of SCLK and sends the data on the falling edge of SCLK.

Start flag means DIO is in the falling edge while SCLK is high.

Stop flag means DIO is in the rising edge while SCLK is high.

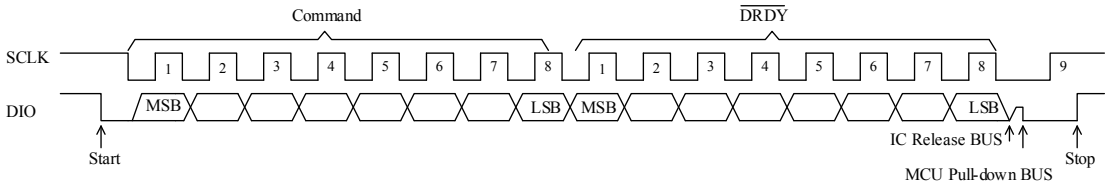
Specific command sequence chart and analysis are as follows:

a) Write to setup register



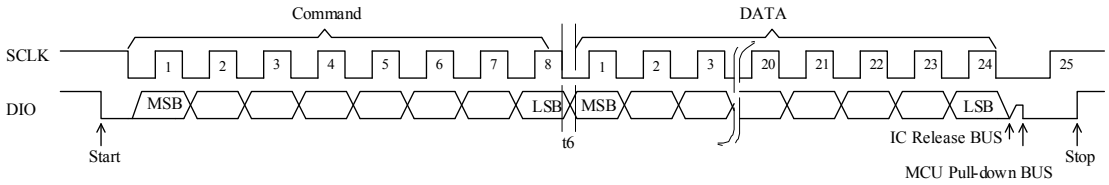
First issue start flag, then issue 8-bit BF command followed by issuing 8-bit data to be written in the setup register, at last issue stop flag.

b) Read access to DRDY command



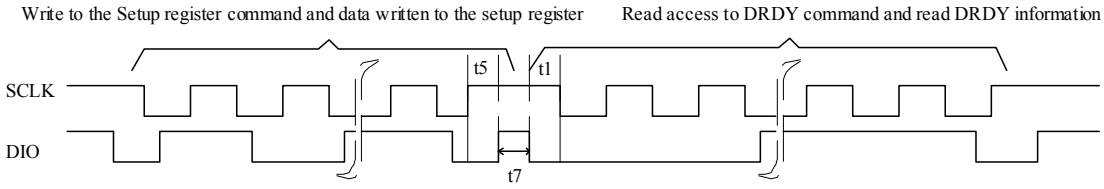
First issue start flag, then issue 8-bit 3F command followed by issuing 8 data read from the SCLK clock, at last issue stop flag.

c) Read access to data register



First issue start flag, then issue 8-bit 7F command followed by issuing 24 data read from the SCLK clock, at last issue stop flag.

d) Multiples of command sequence



Note: the above communication sequences must be strictly followed in communication

(4) Sequence characteristics:

(Refer to the communication sequence chart)

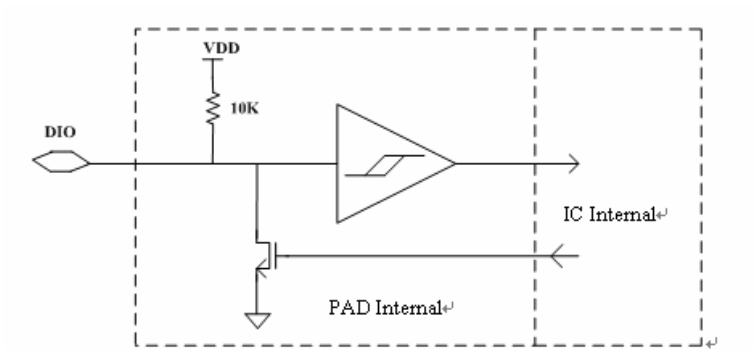
Parameter	Value (T_{MIN},T_{MAX})	Units	Conditions/Comments
t1	100(T_{MIN})	ns	Start flag to SCLK pull-down
t2	100(T_{MIN})	ns	SCLK high pulsewidth
t3	100(T_{MIN})	ns	SCLK low pulsewidth
t4	100(T_{MIN})	ns	the last SCLK pulse to SCLK pull-up time
t5	100(T_{MIN})	ns	SCLK Pull-up to stop flag time
t6	100(T_{MAX})	ns	SCLK falling edge to data output time
t7	100(T_{MIN})	ns	Time among commands when SCLK and DIO is high

(5) Electrical characteristics: (All logic Input)

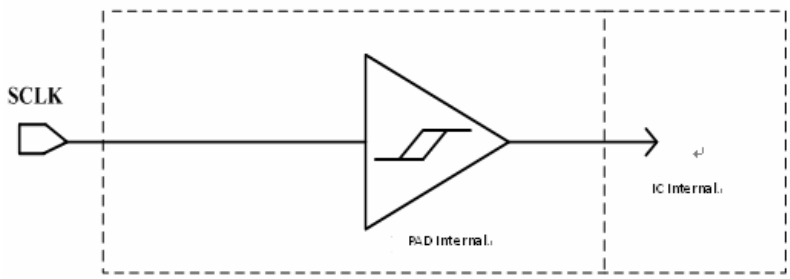
Parameter	Value	Units	Conditions/Comments
V_{T+}	1.286	V	VDD=3V Nominal
V_{T-}	0.734	V	VDD=3V Nominal
V_{T+}	1.633	V	VDD=5V Nominal

(6) Introduction to the internal structure of the pin in the communication port:

a) DIO pin



b) SCLK pin



V Output noise

(1) The output noise of the TM7709 at 5V

Table 5_1 shows the output rms noise and effective resolution of the TM7709 when fCLKIN=4.9152MHZ (or an internal oscillator is used). The given data are applied to bipolar input range with a VREF of +2.5V. These data are typical and are generated at an analog input voltage of 0V. The data within the brackets in every table are the effective resolution of the device (rounded to the nearest 0.5LSB). The effective resolution of the device is defined as the ratio between the output rms noise and the input full scale (e.g. 2×VREF/GAIN). It should be noted that they are not calculated based on the peak-to-peak output noise data. The peak-to-peak noise data can be up to 6.6 times of RMS data, at the same time, the effective resolution data based on peak-to-peak noise can be lower 2.5 bits those that based on rms noise as shown in the brackets in the table.

Filter First Notch and O/P Data Rate	Typical Output RMS Noise in μ V(Valid Resolution in bits)	
	Gain of 16	Gain of 128
10Hz	0.17 (21)	0.14 (18)

Table 5_1 Output noise/resolution and gain of the TM7709 (voltage: 5V)

(2) The output noise of the TM7709 at 3V

Table 5_2 shows the output rms noise and effective resolution of the TM7709 when fCLKIN=4.9152MHZ (or an internal oscillator is used). The given data are applied to bipolar input range with a VREF of +1.25V. These data are typical and are generated at an analog input voltage of 0V. The data within the bracket in every table are the effective resolution of the device (rounded to the nearest 0.5LSB). The effective resolution of the device is defined as the ratio between the output RMS noise and the input full scale (e.g. 2×VREF/GAIN). It should be noted that they are not calculated based on the peak-to-peak output noise data. The peak-to-peak noise data can be up to 6.6 times of rms data, at the same time, the effective resolution data based on peak-to-peak noise can be lower 2.5 bits than those based on rms noise as shown in the brackets in the table.

Filter First	Typical Output RMS Noise in μ V(Effective resolution in bits)	
Filter First Notch and O/P	Gain of 16	Gain of 128
10Hz	0.2 (19.5)	0.2 (16.5)

Table 5_2 Output noise/resolution and gain of the TM7709 (voltage: 3V)

VI Analog Input

(1) Analog input range:

The TM7709 includes an analog input pair AIN1+ and AIN1-. This input pair provides a programmable gain and differential input channel which can handle either unipolar or bipolar input signals. It should be noted that the bipolar input signals are referenced to the respective AIN1- input of the input pair. The common-mode range of the input is from GND to VDD provided that the absolute value of the analog input voltage lies between GND -30mV and VDD+30mV. This means that the device can handle both unipolar and bipolar input signals from all gains.

(2) Reference input:

REFIN+ provides reference input for the TM 7709. The reference voltage range is from VDD to 1.0V. The TM7709 is functional with VREF down to below 1.0V, but the output noise will get larger with degraded performance.

To further reduce the noise level, it is generally suggested that a de-coupling capacitor should be applied to the reference voltage input pin.

VII System clock and AD data updating rate

(1) System Clock:

The system clock of the TM 7709 is provided by an internal oscillator, which has an output frequency of 5M. It is a high-precision oscillator which has ultra low dependence on VDD and temperature.

(2) AD data updating rate:

When the system clock is 5M Hz, AD data updating rate f_{AD} is 10.17Hz.

So the calculation formula of f_{AD} is as follows:

$f_{AD} = (f_{CLK}/5) * 10.17$ among which, f_{CLK} refers to the system clock.

VIII Calculation of the input voltage

The data updating rate is about 10Hz in the data conversion, as represented through DRDY signal. The DRDY signal is low, which indicates that a new output word is available from the TM7709 data register. The DRDY pin returns high upon completion of a read operation of a full output word. If no data read occurs between the two output updates, the DRDY will return high for 500 $\times t_{CLKIN}$ prior to the next output update. While DRDY is high, a read operation should not be attempted or in progress to avoid reading from the data register as it is being updated. The DRDY returns low again when the data is updated.

The output data is D2F000H (13824000d) at a positive full scale input voltage; (Ignore the op-amp offset)
The output data is 697800H (6912000d) at a zero input voltage; (Ignore the op-amp offset)
The output data is 000000H (0d) at a negative full scale input voltage; (Ignore the op-amp offset)

$$V_{in} = \frac{Vref}{gain} \times \frac{data - 6912000}{13824000/2}$$

Among which, V_{in} is the channel input voltage, V_{ref} is the reference voltage, gain is the set gain value, and data is the read data in the data register.
In consideration of the offset, the accurate calculation of gain calibration is:
(1) Set the input voltage of the channel to be tested is 0V, when 0V is read, the corresponding AD output data is Z.
(2) Set the input voltage of the channel to be tested is a full scale of FV, when FV is read, the corresponding AD output data is B.
So V_x is applied to the channel to be tested, the calculation formula is as follows:

$$Vx = \frac{(F-0)V}{B-Z} \times (X-Z)$$

Among which, X is the corresponding AD output data when V_x is applied to the channel to be tested.

IX Power consumption

The power consumption of the TM7709 in every status is as follows:

Operating Voltage **VDD**	Chip Status	Method for providing system clock	Total current of the chip $\mathbf{I_{vdd}}$
3V	Normal operation	Internal Oscillator (about 5M Hz)	415μA
3V	Standby mode	Internal Oscillator	3.2μA
5V	Normal operation	Internal Oscillator （about 5M Hz）	605μA
5V	Standby mode	Internal Oscillator	10.6μA

X The use notice of the TM 7709

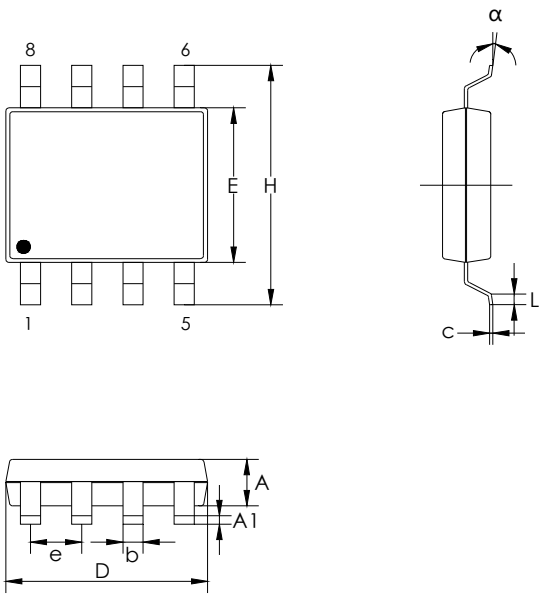
(1) Standby mode

The STBY bit in the setup register allows users to place the device in a Power-down Mode when it is not required to provide AD conversion results. In the standby mode, the TM7709 retains all the contents of all its on-chip registers (including setup register and data register). When released from standby mode, the device starts to process data and a valid new word is available in the data register in 3 ×1/output rate from when a 0 is written to the STBY bit.

The STBY bit does not affect the digit interface, and it does not affect the status of the DRDY bit. If DRDY is high when the STBY is brought low, it will remain high until there is a valid new word in the data register. If DRDY is low when the STBY bit is brought low, it will remain low until the data register is updated. If DRDY is low when the device enters its standby mode (indicating that a valid unread word in the data register), the data register can be read while the device is in standby. At the end of this read operation, the DRDY will be reset high as normal.

The device, in its standby mode, has very low power consumption. Please refer to the power consumption section for the specific parameters.

XI Package:



	Dimensions In Inches			Dimensions In Millmeters		
symbol	**Min**	**Nom**	**Max**	**Min**	**Nom**	**Max**
A	0.051	0.059	0.067	1.30	1.50	1.70
A1	0.002	0.006	0.010	0.06	0.16	0.26
b	0.012	0.016	0.022	0.30	0.40	0.55
c	0.006	0.010	0.014	0.15	0.25	0.35
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.163	3.75	3.95	4.15
e		0.050			1.27	
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.018	0.026	0.033	0.45	0.65	0.85
α	0°		8°	0°		8°

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