BUCKET BRIGADE DELAY LINE FOR ANALOGUE SIGNALS

The TDA1022 is a MOS monolithic integrated circuit, generally intended to delay analogue signals (e.g. delay time = 512/2 f₀).
It can be used with clock frequencies in the range 5 kHz to 500 kHz.
The device contains 512 stages, so the input signal can be delayed from 51.2 ms to 0.512 ms.
Applications in which the device can be used:
- variation of fixed delays of analogue signals, vox control, equalizing speech delay in public address systems;
- in electronic organs and other musical instruments for vibrato and chorus effects;
- reverberation effects;
- variable compression and expansion of speech in tape-recorders;
- in communication systems for speech scrambling and time scale conversion.

<table>
<thead>
<tr>
<th>QUICK REFERENCE DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (pin 9)                      VDD  nom.    -15    V</td>
</tr>
<tr>
<td>Clock frequency                          f₀        5 to 500 kHz</td>
</tr>
<tr>
<td>Number of stages                        512</td>
</tr>
<tr>
<td>Signal delay range                     tₐd        51.2 to 0.512 ms</td>
</tr>
<tr>
<td>Signal frequency range                  fₛ         0 (d.c.) to 45 kHz</td>
</tr>
<tr>
<td>Input voltage at pin 5 (peak-to-peak value) V₅-16(p-p) typ. 7 V</td>
</tr>
<tr>
<td>Line attenuation                      V₅-16(p-p) typ. 4 dB ¹)</td>
</tr>
</tbody>
</table>

PACKAGING OUTLINE  plastic 16-lead dual in-line (see general section).

¹) See note 1 on page 4.
CIRCUIT DIAGRAM

PINNING
1. Clock input 1 (V_{CL1})
2. Not connected
3. Not connected
4. Clock input 2 (V_{CL2})
5. Signal input
6. Not connected
7. Not connected
8. Output 513
9. Negative supply (V_{DD})
10. Not connected
11. Not connected
12. Output 512
13. Tetrode gate (V_{13-16})
14. Not connected
15. Not connected
16. Ground (substrate)
RATINGS  Limiting values in accordance with the Absolute Maximum System (IEC 134)

Volatages  (see note)

Supply voltage \( V_{9-16} \) 0 to -20 \( V \)
Clock input, data input, output voltage and \( V_{13-16} \) 0 to -18 \( V \)

Current

Output current \( I_8; I_{12} \) 0 to 5 \( mA \)

Temperatures

Storage temperature \( T_{STG} \) -40 to +150 \( ^{\circ}C \)
Operating ambient temperature \( T_{AMB} \) -20 to +85 \( ^{\circ}C \)

Note

Though MOS integrated circuits incorporate protection against electrostatic discharge, they can nevertheless be damaged by accidental over-voltages. To be totally safe, it is desirable to take handling precautions into account.

CHARACTERISTICS  at \( T_{AMB} = -20 \) to +55 \( ^{\circ}C \); \( V_{DD} = -15 \) \( V \); \( V_{\phi L} = V_{\phi 2} = -15 \) \( V \);
\( V_{13-16} = -14 \) \( V \); \( R_L = 47 \) \( k\Omega \) (unless otherwise specified)

Supply voltage range \( V_{DD} \) -10 to -18 \( V \) 1)
Supply current \( I_9 \) typ. 0,3 \( mA \)
Clock frequency \( f_1; f_2 \) 5 to 500 \( kHz \) 2)
Clock pulse width \( t_{\phi 1} ; t_{\phi 2} \) \( \geq \) 0,5 \( T \) 3)
Clock pulse rise time \( t_{\phi 1r} ; t_{\phi 2r} \) typ. 0,05 \( T \) 3)
Clock pulse fall time \( t_{\phi 1f} ; t_{\phi 2f} \) typ. 0,05 \( T \) 3)
Clock pulse voltage levels; HIGH \( V_{\phi H} \); \( V_{\phi 2H} \) 0 to -1,5 \( V \)
LOW \( V_{\phi 1L} ; V_{\phi 2L} \) typ. -15 \( V \) 1)

Signal input voltage at 1% output voltage distortion (r.m.s. value) \( V_{S(rms)} \) typ. 2,5 \( V \)
Signal frequency \( f_s \) 0 (d.c.) to 45 \( kHz \)

1) It is recommended that \( V_{13-16} = V_{\phi 1L} + 1 \) \( V \) = \( V_{\phi 2L} + 1 \) \( V \); \( V_{DD} \) more negative than \( V_{\phi L} \).
2) In theory the clock frequency must be higher than twice the highest signal frequency; in practice \( f_s \leq 0,3 f_{\phi} \) to 0,5 \( f_{\phi} \) is recommended, depending on the characteristics of the output filter.
3) \( T = \) period time = \( 1/f_{\phi} \). The data on fall and rise times are given to eliminate overlap between the two clock pulses. To be independent of these rise and fall times a clock generator with simple gating can be used. See also pages 5 and 8.
CHARACTERISTICS (continued)

Attenuation from input to output
\( f_0 = 40 \text{ kHz}; \ f_s = 1 \text{ kHz} \)

<table>
<thead>
<tr>
<th></th>
<th>typ.</th>
<th></th>
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</thead>
<tbody>
<tr>
<td></td>
<td>4 dB</td>
<td>&quot;</td>
</tr>
<tr>
<td>&lt;</td>
<td>7 dB</td>
<td>1</td>
</tr>
</tbody>
</table>

Change in output at \( f_s = 1 \text{ kHz} \): \( V_s(\text{rms}) = 1 \text{ V} \)
when \( f_0 \) varies from 5 to 100 kHz

<table>
<thead>
<tr>
<th></th>
<th>typ.</th>
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<tbody>
<tr>
<td></td>
<td>0.5 dB</td>
<td>&quot;</td>
</tr>
<tr>
<td>&lt;</td>
<td>1 dB</td>
<td>&quot;</td>
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</table>

when \( f_0 \) varies from 100 to 300 kHz

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<tr>
<th></th>
<th>typ.</th>
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<tr>
<td></td>
<td>0.5 dB</td>
<td>&quot;</td>
</tr>
<tr>
<td>&lt;</td>
<td>1 dB</td>
<td>&quot;</td>
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D.C. voltage shift when \( f_0 \) varies from 5 to 300 kHz

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<thead>
<tr>
<th></th>
<th>typ.</th>
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<tbody>
<tr>
<td></td>
<td>0.5 V</td>
<td>&quot;</td>
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</table>

Noise output voltage (r.m.s. value)
\( f_0 = 100 \text{ kHz} \) (weighted by "A" curve)

<table>
<thead>
<tr>
<th></th>
<th>typ.</th>
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<tbody>
<tr>
<td></td>
<td>0.25 mV</td>
<td>&quot;</td>
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Signal-to-noise ratio at max. output voltage

<table>
<thead>
<tr>
<th></th>
<th>typ.</th>
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<tr>
<td></td>
<td>74 dB</td>
<td>&quot;</td>
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Load resistance

<table>
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<tr>
<th></th>
<th>typ.</th>
<th></th>
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<tbody>
<tr>
<td></td>
<td>47 kΩ</td>
<td>&quot;</td>
</tr>
</tbody>
</table>

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1) Attenuation can be reduced to typ. 2.5 dB if load resistor is replaced by a current source of 100 to 400 \( \mu \text{A} \).
Adjust d.c. voltage for class-A operation (±5 V).

Conditions: low pass filter μA741CV (12 dB per octave);

*gain = +3.5 dB (compensation for line attenuation);

\[ f_0 = 50 \text{ kHz (min.)}; \]

**cut-off frequency = 15 kHz.
APPLICATION INFORMATION (continued)

Series connection of two lines TDA1022

*) Adjust d.c. voltage for class-A operation (≈ 5 V).

**) Clock input voltage amplitude: $V_{CL} = -15$ V.

***) Can be replaced by a current source of 100 to 400 μA (see also note 1 on page 4).
VDD = 0
VSS = -15 V
f_\phi = 15 kHz

Clock oscillator and driver circuit with elimination of overlap (for max. 6 x TDA1022)
Conditions for the graph above:
V_{DD} = -15\, \text{V}
V_{13-16} = -14\, \text{V}
V_{\phi H} = 0\, \text{V}
f_{\phi} = 40\, \text{kHz}
R_L = 47\, \text{k}\, \Omega

Conditions for the left-hand graph:
V_{DD} = -15\, \text{V}
V_{13-16} = -14\, \text{V}
V_{\phi H} = 0\, \text{V}
f_{\phi} = 40\, \text{kHz}
f_s = 1\, \text{kHz}
R_L = 47\, \text{k}\, \Omega
Conditions for the graph above:
V_{DD} = -15 V
V_{13-16} = -14 V
V_{\phi} = 0 \text{ to } -15 V

Conditions for the left-hand graph:
\text{f}_{S} = 1 \text{ kHz}
V_{S} = -5.2 \text{ V}
V_{DD} = -15 \text{ V}
V_{13-16} = -14 \text{ V}
V_{\phi} = 0 \text{ to } -15 V
\text{f}_{\phi} = 40 \text{ kHz}