LD3320

Datasheet

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ICRoute 用声音去沟通
VUI (Voice User Interface)

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1. Introduction

The LD3320 chip is a speech recognition chip designed and produced by ICRoute. The chip integrates a speech recognition processor and some external circuits, including AD, DA converters, microphone interfaces, and sound output interfaces. The chip is designed with emphasis on energy efficiency and high efficiency, and does not require any external auxiliary chips such as Flash, RAM, etc. The direct integration into existing products enables voice recognition/voice control/human-machine dialogue functions. And, the identified keyword list can be dynamically edited. (For other technical information, please visit www.icroute.com to read and download)

2. Features

The main features are:

Non-specific human voice recognition is accomplished through ICRoute's unique fast and stable optimization algorithm. Users do not need prior training and recording. The recognition accuracy rate is 95%.

It is not necessary to connect any auxiliary Flash chip, RAM chip and AD chip to complete the voice recognition function. Really provides a single-chip speech recognition solution.

A maximum of 50 candidate recognition sentences can be set for each recognition. Each recognition sentence can be a single word, phrase, or short sentence. The length is no more than 10 Chinese characters or 79 bytes of Pinyin. On the other hand, the identification sentence content can be dynamically edited and modified, so a system can support multiple scenarios.

A 16-bit A/D converter, 16-bit D/A converter, and power amplifier circuit have been prepared inside the chip. Microphones, stereo headphones, and monaural speakers can be easily connected to the chip pins. The output power of the stereo headphone jack is 20mW, and the output power of the horn interface is 550mW, which can produce clear and loud sound.

Parallel and serial interfaces are supported. The serial mode can simplify the connection with other modules.

Can be set to sleep state and can be easily activated.

MP3 playback function is supported. No external auxiliary device is required. The main control MCU sends MP3 data to the LD3320 chip in sequence to output the sound from the corresponding PIN of the chip. Product design can choose from stereo headphones or mono speakers to get the sound output. Supports MPEG1 (ISO/IEC11172-3), MPEG2 (ISO/IEC13818-3) and MPEG 2.5 layer 3 formats.

- Power supply is 3.3V, if used in a portable system, use 3 AA batteries to meet

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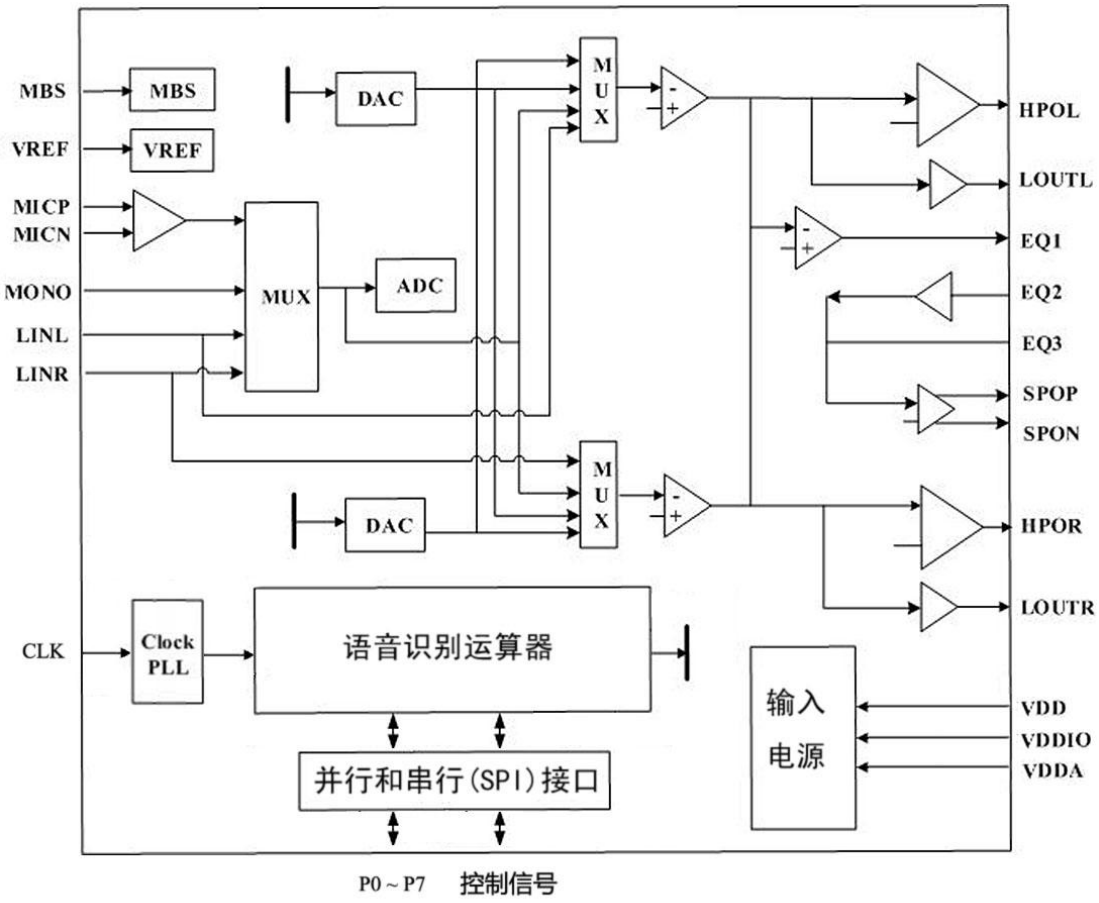
3. Circuit description

The following is a simple logic diagram of the internal circuit.



Details are as follows:

Voltage requirements

VDD	Digital circuit power input	3.0 V - 3.3 V
VDDIO	Power input for digital I/O circuit	1.65 V - VDD
VDDA	Power input for analog circuit	3.0 V - 4.0 V

It is recommended that users can use a unified 3.3v voltage input to simplify the design. Separating the digital voltage from the analog voltage can make the chip better.
Chip pin input voltage range:
High voltage (logic "1"): 0.7*VDDIO ~ VDDIO
Low voltage (logic "0"): 0 ~ 0.3*VDDIO
Therefore, the developer needs to ensure that the master MCU he uses works in the same way as 3.3v, ensuring that the high voltage output from the master MCU to the LD3320 does not exceed 3.3V.

Clock

The chip must be connected to an external clock with an acceptable frequency range of 4 to 48 MHz. There is also a PLL frequency synthesizer inside the chip that can generate specific frequencies for use by internal modules.

Reset

The reset signal (RSTB*) to the chip must be made after VDD/VDDA/VDDIO is stable. No matter what operation the chip is performing, the reset signal can restore it to the initial state and reset each register. If there is no subsequent instruction (setting of the register), the chip will go to sleep after reset. After this, a CSB* signal can reactivate the chip into working condition.

Parallel interface

The chip can be connected to an external host CPU in parallel, using 8 data lines (P0-P7), 4 control signals (WRB*, RDB*, CS*, A0), and an interrupt return signal (INTB*)).

Serial interface

The serial interface is connected to the external host CPU via the SPI protocol. First connect MD to high level and ground (SPIS*) first. Only 4 pins are used at this time: chip select (SCS*), SPI clock (SDCK), SPI input (SDI), and SPI output (SDO).

Registers

The settings and commands to the chip, including the transfer of data and the acceptance of data, are accomplished through register manipulation. For example, when performing voice recognition, a list of recognized keyword words is set, and a chip recognition mode is set. After the recognition is completed, the recognition result is obtained by reading/writing a register. When the sound is played, the MP3 format data is looped into the FIFO corresponding register. (The recognition result is that the index number of the identified keyword in the keyword list is returned by the register, and the index value is specified when the keyword list is set)

External control of speaker volume

In addition to specific registers to control the volume, circuits outside the chip can control the volume gain of the horn. The pins corresponding to EP1, EP2, and EP3 are used. See Appendix B for details.

Rapid development and evaluation verification

To facilitate developers' rapid development and evaluation of LD3320 chips, ICRoute provides development boards and modules. Developers can refer to the "B-LD3320 Development Board" and "M-LD3320 Module" on the official website for rapid development and verification.

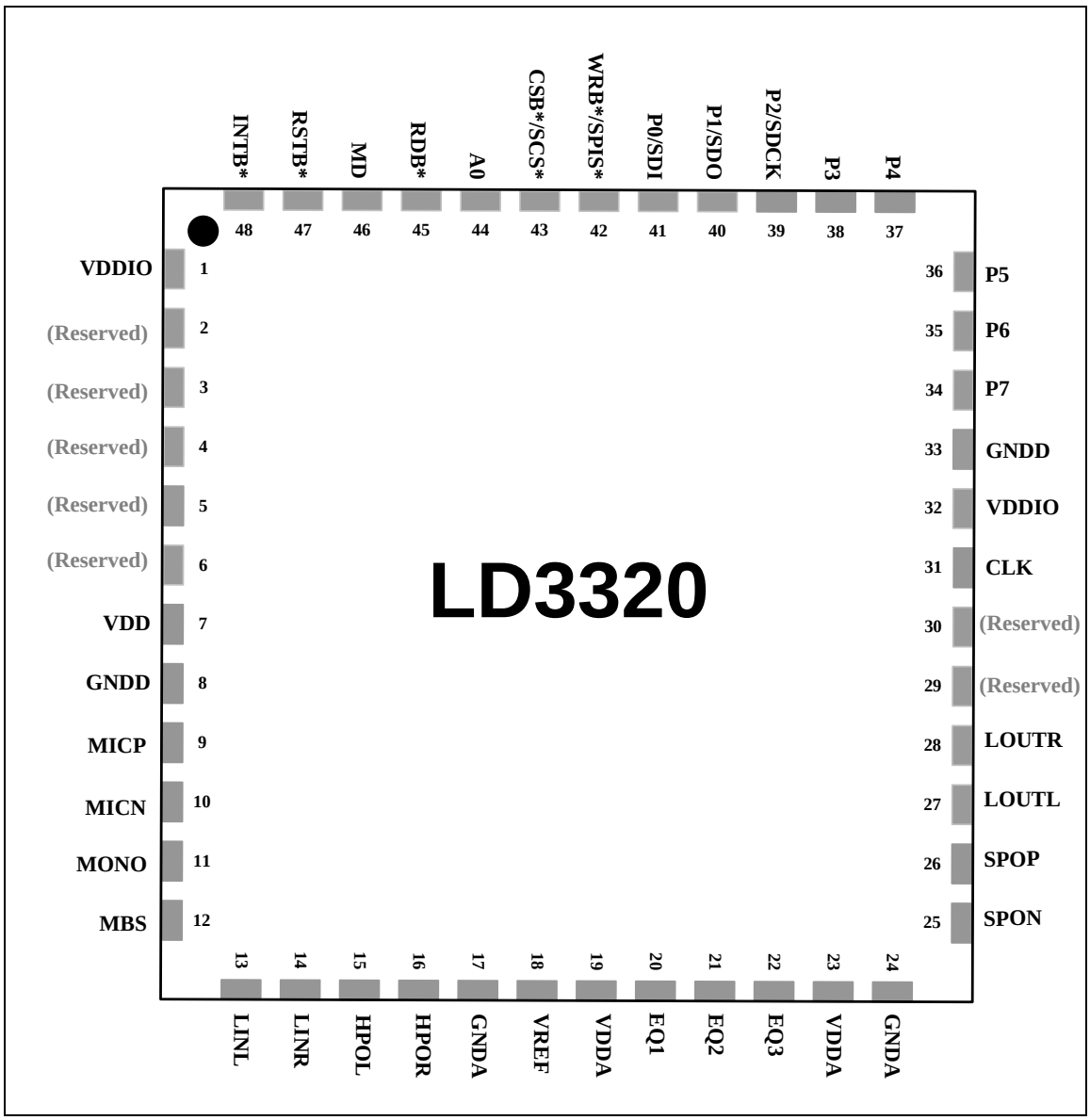
4. Pin description

管脚编号	名称	IO 方向	AD 分类	说明
1，32	VDDIO	–	–	Power Input for Digital I/O Circuits
2	(Reaserved)	–	–	(Connect the pull-up resistor according to the circuit schematic)
3	(Reaserved)	–	–	(Connect the pull-up resistor according to the circuit schematic)
4	(Reaserved)	–	–	(Connect the pull-up resistor according to the circuit schematic)
5	(Reaserved)	–	–	(Connect the pull-up resistor according to the circuit schematic)
6	(Reaserved)	–	–	(Can be left empty)
7	VDD	–	D	Digital logic circuit power supply
8，33	GNDD	–	D	Grounding for IO and digital circuits
9，10	MIC[P, N]	I	A	Microphone input (positive and negative)
11	MONO	I	A	Mono LineIn input
12	MBS	–	A	Microphone bias
13，14	LIN[L, R]	I	A	Stereo LineIn (left and right ends)
15，16	HPO[L, R]	0	A	Headphone output (left and right ends)
17	GNDA	–	A	Ground for analog circuits
18	VREF	–	A	Sound signal reference voltage
19，23	VDDA	–	A	Analog signal power supply
20	EQ1	0	A	Speaker volume external control 1
21	EQ2	I	A	Speaker volume external control 2
22	EQ3	0	A	Speaker volume external control 3
24	GNDA	–	A	Ground for analog circuits
25，26	SPO[N, P]	0	A	Speaker output
27，28	LOUT[L, R]	0	A	LineOut output
29	(Reaserved)	–	–	(Refer to the instructions in Appendix B.4)
30	(Reaserved)	–	–	(Refer to the instructions in Appendix B.4)
31	CLK	I	D	Clock input 4 - 48 (MHz)
34	P7	I/O	D	Connect parallel port (bit 7) to pull-up resistor
35	P6	I/O	D	Connect parallel port (bit 6) to pull-up resistor
36	P5	I/O	D	Connect parallel port (bit 5) to pull-up resistor
37	P4	I/O	D	Connect parallel port (bit 4) to pull-up resistor
38	P3	I/O	D	Connect parallel port (bit 3) to pull-up resistor
39	P2/SDCK	I/O	D	Parallel port (bit 2), common SPI clock connected to pull-up resistor
40	P1/SDO	I/O	D	Parallel port (bit 1), shared SPI output connect pull-up resistor

41	P0/SDI	I/0	D	Parallel port (bit 0), shared SPI input connected to pull-up resistor
42	WRB*/SPIS*	I	D	Write enable (active low) Shared SPI Enable (Active Low) Connects Pullup Resistors
43	CSB*/SCS*	I	D	Parallel Chip Select Signals, Shared SPI Chip Select Signals Connected to Pull-up Resistors
44	A0	I	D	Address or data selection. When WRB* is active, high indicates that P0~P7 is the address, and low indicates that P0~P7 are data. Connect pull-up resistor
45	RDB*	I	D	Read Enable (Active Low) Connect Pullup Resistors
46	MD	I	D	0: Work in parallel 1: Serial operation mode (SPI protocol) Connected pull-up resistor
47	RSTB*	I	D	Reset signal (active low) Connect pull-up resistor
48	INTB*	0	D	Interrupt output signal (active low) Connect pull-up resistor
共 48 个				

Explanation:
IO Direction: I indicates input; O indicates output.
AD Classification： A indicates an analog signal; D indicates a digital signal.

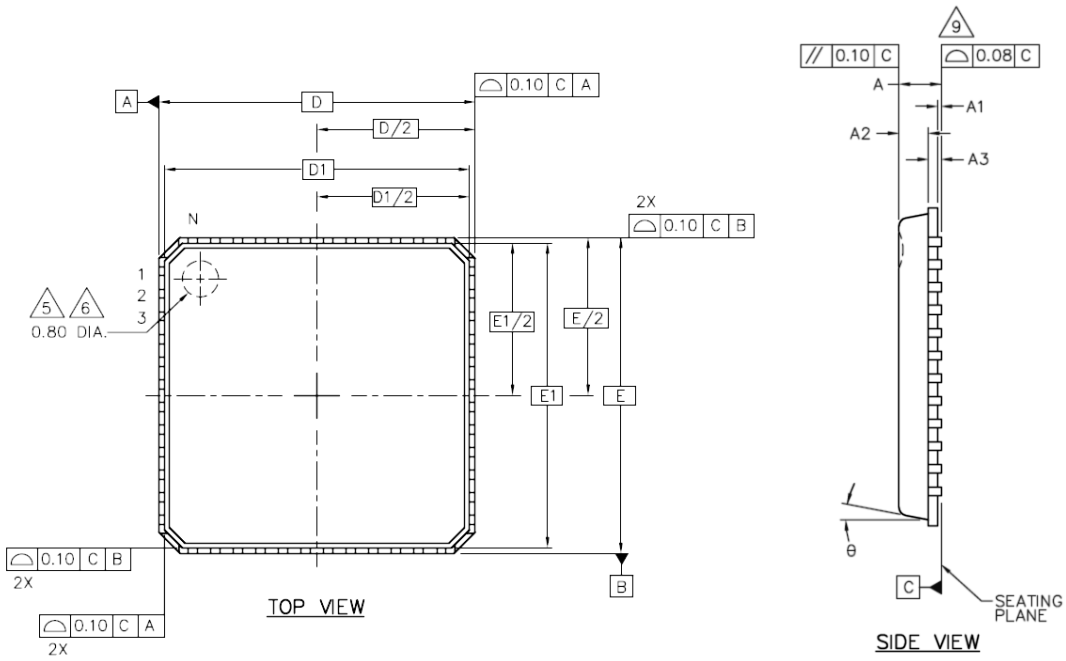
Pins are distributed as shown below:

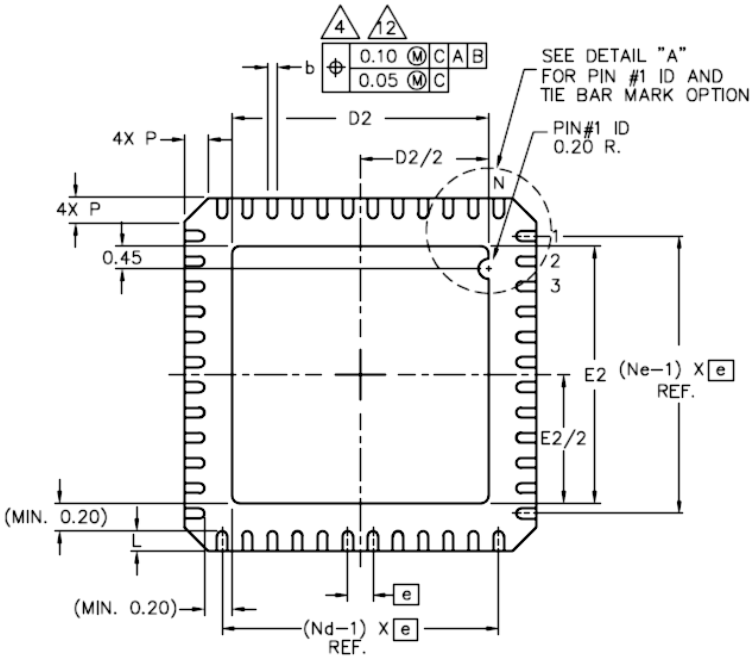


Appendix A Package Appearance

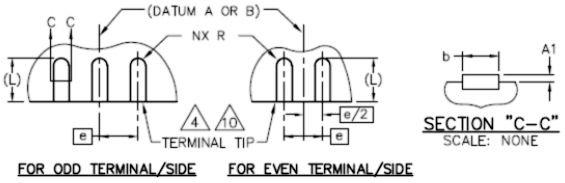
The chip is packaged in a 48-pin QFN plastic package. The size is approximately 7*7*0.85 mm. The package is small and the pins are arranged properly. The figure below shows the actual image on the front of the package.

Detailed dimensions are described as follows: chip pin pitch 0.5mm

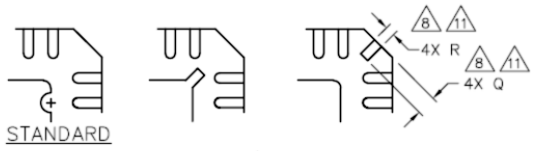




BOTTOM VIEW



FOR ODD TERMINAL/SIDE FOR EVEN TERMINAL/SIDE

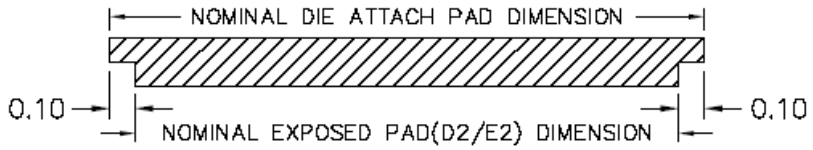


DETAIL "A" – PIN #1 ID AND TIEBAR MARK FIGURES

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	10
A2	0.60	0.65	0.70	
A3		0.20 REF.		
D		7.00 BSC		
D1		6.75 BSC		
E		7.00 BSC		
E1		6.75 BSC		
θ	0	–	12°	
P	0.24	0.42	0.60	
Q	0.30	0.40	0.65	8,11
R	0.13	0.17	0.23	8,11

SYMBOL	PITCH VARIATION			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		48		3
Nd		12		3
Ne		12		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	5.40	5.50	5.65	
E2	5.40	5.50	5.65	

GENERAL ; NOMINAL EXPOSED PAD(D2/E2) DIMENSION
NOMINAL DIE ATTACH PAD DIMENSION−0.20



<DIE ATTACH PAD X−SECTION VIEW>

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM(.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. − 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X−DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y−DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
10. APPLIED ONLY FOR TERMINALS.
11. Q AND R APPLIES ONLY FOR STRAGHT TIEBAR SHAPES.
12. FOR 0.40mm LEAD PITCH, THE LEAD POSITION TOLERANCE MUST BE 0.07mm AT THE ACTUAL MEAN VALUE OF BODY SIZE.
13. MOLD FLASH OR PLATING COVERAGE ON THE RING PAD AREA SHALL BE ALLOWABLE

Appendix B. Auxiliary Circuits

1. **External control of speaker volume**

The external circuit can change the volume of the speaker. For example, the resistance values of the resistors R6 and R2 in the figure below are 33K and 15K respectively. Then 33/15=2.2, the sound is amplified about 2 times. If you connect a variable resistor to R6, you can adjust the volume manually.

It is recommended that the user adopt a circuit similar to that of Figure B-1.

2. **Microphone biased auxiliary circuit**

Pin 12 (MBS) is a microphone bias and requires an RC circuit to ensure that it can output a floating voltage to the microphone. It is recommended that the user adopt a circuit similar to that shown in Figure B-2.

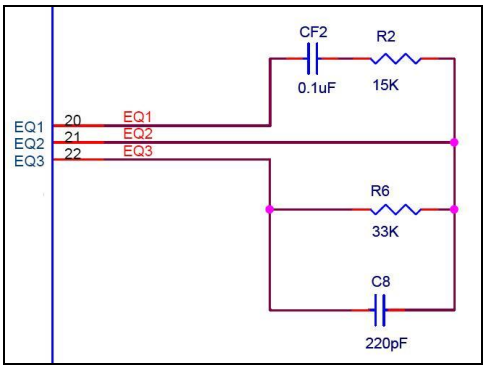


Figure B-1
External Control of Speaker Volume

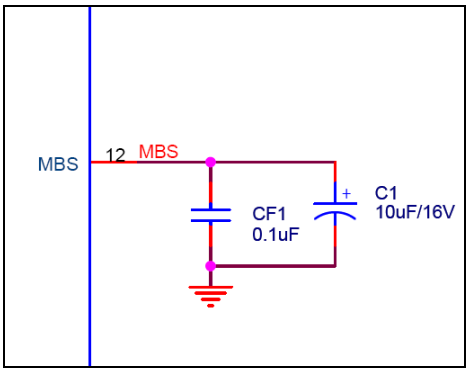


Figure B-2
Auxiliary circuit for microphone gain

3. The correct welding pull-up resistor assists the stable operation of the system

"LD3320 Test Board Schematic" gives the recommended pull-up resistors, including P0~P7, MD, RDB, CSB, INTB, WRB, RSTB, A0 and other control pins connected to 1k/10k pull-up resistors. The user also tries to solder the pull-up resistor to ensure that the signal of the chip control port is stable and the auxiliary system works stably.

4. **The pins of the chip's analog signal need to be properly soldered to the auxiliary circuit.**

"LD3320 Test Board Schematic" shows the peripheral auxiliary circuits of the analog signal pins of the chip, including Audio Input; Audio Output; External control circuit of EQ1/EQ2/EQ3 speaker volume; Auxiliary circuit of analog power supply and so on. The designer must be able to properly solder these auxiliary circuits based on the capacitance/resistor devices given in the "LD3320 Test Board Schematic" to ensure that the analog module of the chip can operate normally.

5. **Chip Pin 29, Pin 30 Description**

Chip pin 29 and pin 30 will stably output a low voltage after a chip reset (RSTB*). Developers can connect LEDs on these two pins as a power-up indication for the chip (such as the connection shown in "LD3320 Test Board Schematic"). You can also hang these two pins directly.

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