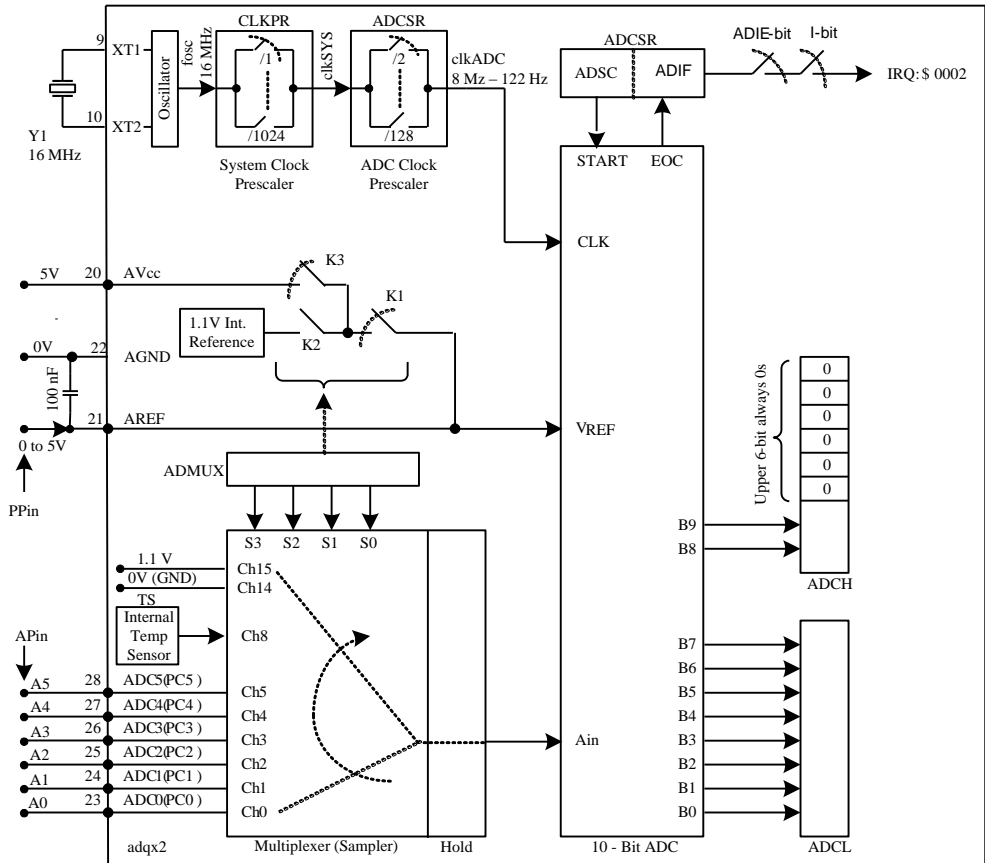


## 4.1 Organization of Analog-to-Digital Converter Module



**Figure-4.1:** Conceptual View of the ADC Module of ATmega328 MCU

- (1) The ATmega328 contains a built-in SAR (successive approximation register)-type multi-channel analog-to-digital converter of which only 6-channels (Ch0 – Ch5) are available to the acquire external signals via APin (analog pin connector: A0 – A5) connector of the Arduino UNO Learning Kit. Ch8, Ch14, and Ch15 are internally connected to ‘Temperature Sensor, TS’, 0V and 1.1 V respectively. The desired channel is selected with the help of ADMUX (ADC Multiplexer Register).
- (2) For this MCU, the input voltage to an external channel must be equal or less than the voltage connected at the  $V_{REF}$  point of the ADC. The ADC can receive its  $V_{REF}$  voltage from three sources: External 5V ( $AV_{cc}$  = Analog Voltage), Internal 1.1 V ( $V_{BG}$  = Band Gap Voltage), and External Variable Voltage ( $AREF$  = 0 to 5V). The usual voltage of the reference point is 5V. We must use 1.1V as  $V_{REF}$  while measuring the signals of Ch8, Ch14, and Ch15.

A warning, extracted from the Arduino Language Reference Manual, is worth to mention: While connecting  $V_{REF}$  point to the external AREF-point, the voltage at the AREF point must not be less than 0V or higher than 5V; otherwise, the MCU will possibly be damaged. The  $V_{REF}$  voltage selection is made via ADMUX register.

- (3) Full Scale (FS) of an ADC: It is the maximum analog input voltage for which all the output bits (B0 – B9) will assume LH states.
- (3) Resolution of an ADC:
  - (a) Assume  $FS = 5V = 5000 \text{ mV}$ .
  - (b) When  $V_{in} = 5000 \text{ mV}$ , the output = 111111111 (1023) =  $2^{10}-1 = 2^n - 1$
  - (c) Resolution =  $5000 \text{ mV}/1023 = 4.8875 \text{ mV}$  for the LS-Bit of the output.
  - (d) Better resolution ADC means: lesser mV for the LS-Bit of the output.
  - (e) According to data sheets, the Resolution:  $5000 \text{ mV}/10^n = 5000/1024 = 4.8821 \text{ mV}$ .
- (4) The following conditions are to be satisfied to transform a port pin of PORTC into an analog channel for the ADC.
  - (a) LL must be written into Bit-0 of the PRR (Power Reduction Register).
  - (b) ADC must be enabled by putting LH at Bit-7 of the ADCSRA-register. The directions of the port pins of PORTC are automatically configured as inputs.
  - (c)  $V_{REF}$  voltage for the ADC and analog channel selection (which channel to acquire) are to be done with the help of ADMUX register.
  - (d) ADC must be started by putting LH at the ADSC (ADC Start Conversion) Bit of the ADCSRA. The conversion time of the ADC :  $13 \mu\text{s} - 260 \mu\text{s}$ .
- (5) End-of-Conversion (EOC) is detected in the following ways:
  - (a) By polling the ADSC bit of ADCSRA and checking that it has assumed LL-state. As long as the conversion is going on, the ADSC bit remains at LH state. At the end-of-conversion ADSC assumes LL state.
  - (b) By polling the ADIF bit of ADCSRA and checking that it has assumed LH-state. As long as the conversion is going on, the ADIF bit remains at LL state. At the end-of-conversion ADIF assumes LH state. If interrupt is made active by enabling the I-bit of SREG and ADIE-bit of ADCSRA, this ADIF-bit will interrupt the MCU notifying the end-of-conversion. The ADIF is automatically cleared when the MCU vectors to ISR (Interrupt Sub Routine) at location 002Ah. If EOC is detected by polling the ADIF, the ADIF bit must be cleared manually by writing LH at this bit position of the ADCSRA register.
- (6) After the conversion, the 10-bit ADC data is available in the following two registers:
  - (a) ADCL [0:7] : ADC Data Register Low (It contains lower 8-bit).
  - (b) ADCH [8:15] : ADC Data Register High (Bit-8, 9 are the part of ADC result; the remaining 6-bit (Bit-10 to Bit-15 are always 0s.).
  - (c) While reading data from the ADC, the lower 8-bit (ADCL) must be read first.
- (7) Registers involved in the ADC Operation:
  - (a) ADCMUX : ADC Multiplexer Selection Register
  - (b) ADCSRA : ADC Control and Status Register A
  - (c) ADCSRB : ADC Control and Status Register B
  - (d) ADCL : ADC Data Register Low

- (e) ADCH : ADC Data Register High
- (f) PRR : Power Reduction Register
- (g) CLKPR: System Clock Prescaler Register