

## Description

DA8620 is an organic light emitting diode (OLED) driver supporting resolutions up to QVGA (240 RGB x 320). DA8620 features Dialog's proprietary SmartXtend™ technology.

SmartXtend can reduce anode peak current and average power consumption without loss of brightness. This improves life time and enables OLED panels to be used as the high resolution main display in mobile phones and other portable devices.

DA8620 integrates all the key functions needed to drive high resolution OLED panels. Its exceptional 0.5% anode source current matching results in a uniform image display. An extended set of digital interfaces allows maximum flexibility for a range of applications. Options include MIPI DBI Type A, B, and C parallel interfaces, 3-wire, 4-wire and 5-wire serial Interfaces and an 18-bit RGB interface, ideal for fast-moving video data. With an integrated oscillator, programmable frame rate, automatic brightness control and an ultra-low standby power mode, the DA8620 is ideal for power sensitive handheld applications.

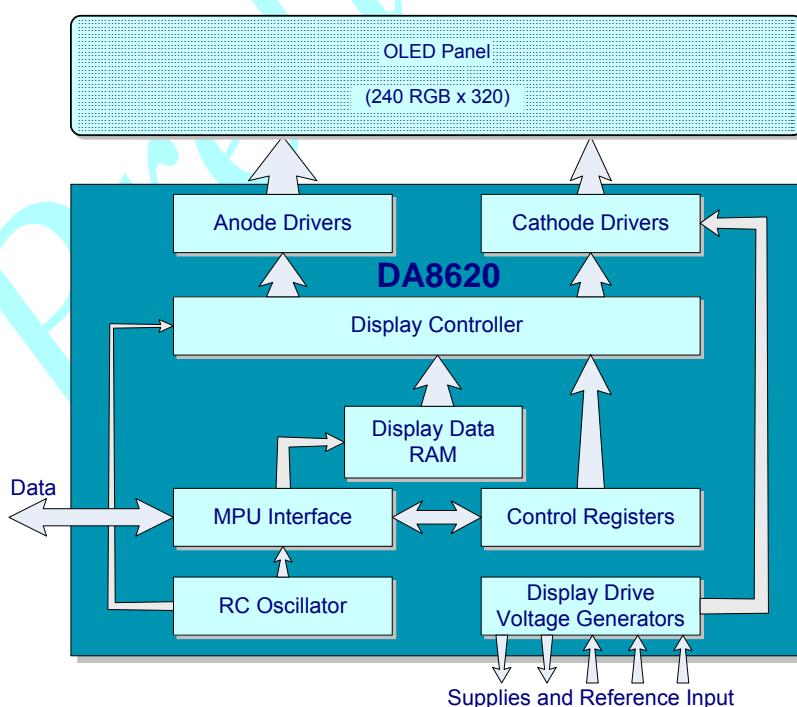
DA8620 is shipped in bare die form with gold bumps, suitable for mounting as chip-on-flex or chip-on-glass.

## Applications

- Mobile phone main display
- Digital still cameras
- PDAs and other hand-held application

## Features

- 240 x 3 (RGB) anode drivers + 320 cathode drivers
- 24 bits RAM: up to 16 M colors
- SmartXtend™ Driving Method (regular single line addressing available)
- Can handle up to 60 frames per second
- 4 factory-loaded Gamma correction curves
- Integrated Oscillator
- Software Enabled Dimmer (divide the luminosity by 2, 4 or 8)
- Automatic and Software Controlled Anode Calibration
- Configurable Cathode Scan Start Position/Direction/Order
- Programmable
  - Duty ratio
  - Frame frequency up to 120 Hz
  - Anode current (for each R, G and B component)
- Ambient light sensing with 10 different brightness levels
- MIPI DBI Type A (68-mode), B (80-mode), and C (options 1,2 & 3) parallel MPU i/f for Register and RAM access
- Serial (3-wire/4-wire/5-wire) Interface for Register and RAM access.
- RGB RAM-only i/f compatible with MIPI DPI (18-bit / 16-bit / 8-bit)
- Suitable for COF and COG implementation



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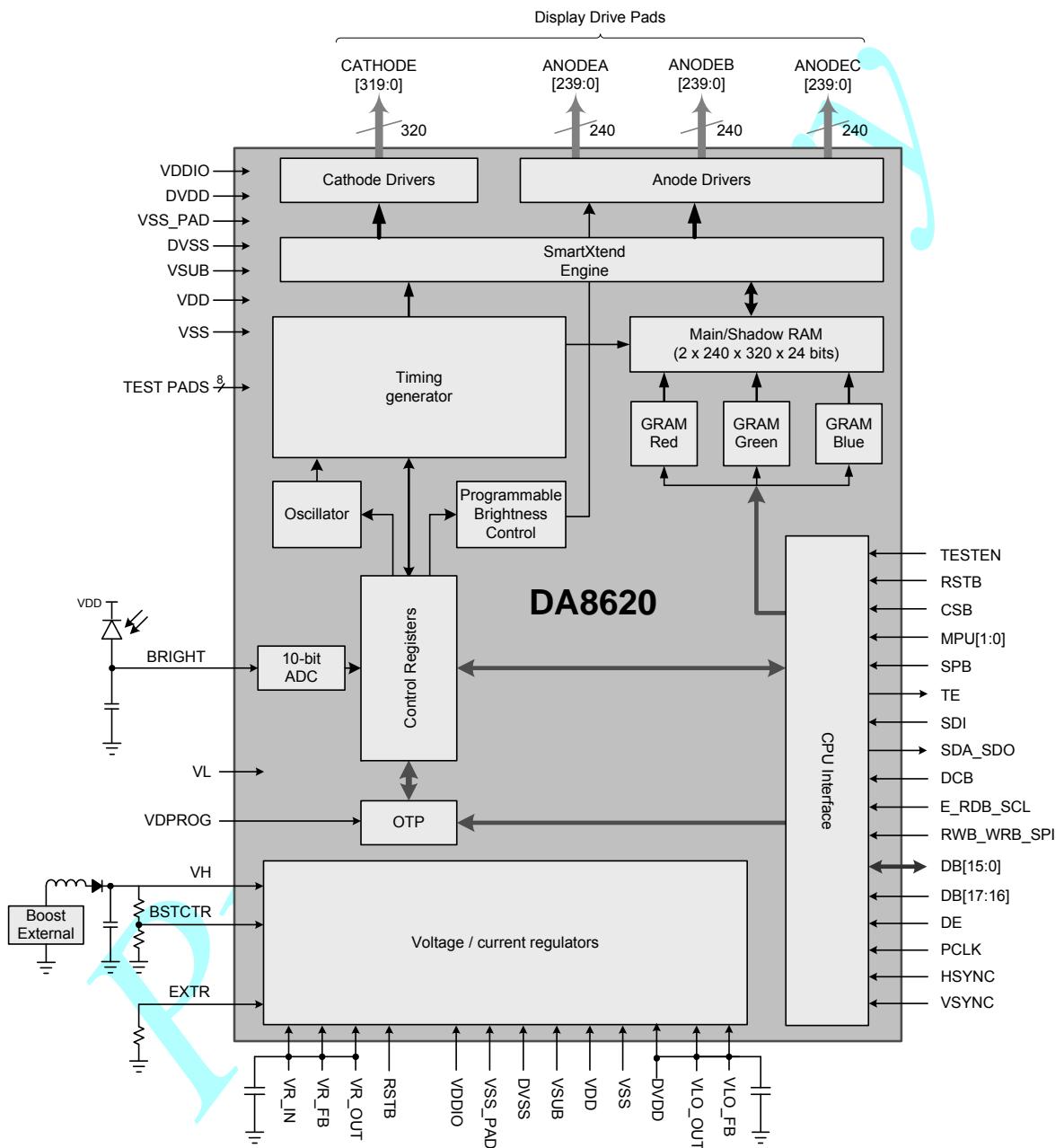
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## 1: Functional Overview

### 1.1 Block Diagram

Figure 1-1: DA8620 Block Diagram



## 1.2 Pad Descriptions

### 1.2.1 Power Supply Pads

Table 1-1: Power Supply Pads

Pad Name	Type	Description	
VDPROG	PWR	Power supply for OTP programming, leave open when not programming (internally diode connected to DVDD)	
VDDIO	PWR	Interface power supply – connect all pads together	
VDD	PWR	Analog power supply – connect all pads together	
VH	PWD	Driver, display, power supply – connect all pads together (multiple groups)	
DVSS	PWR	Digital supply ground – connect all pads together	
VSS	PWR	Analog supply ground – connect all pads together	
VSUB	PWR	Substrate – connect to ground	
VSS_PAD_RIGHT	PWR	Display cathode ground – connect all pads together (multiple groups)	
VSS_PAD_LEFT	PWR	Display cathode ground – connect all pads together (multiple groups)	
VL	PWD	Display anode ground – connect all pads together (multiple groups)	
VR_IN	I	Regulated VR input – connect all pads together	Kelvin connect
VR_FB	I	VR regulator feedback	
VR_OUT	O	VR regulator output – connect all pads together	
DVDD	PWR	Logic Power Supply (1.5 V) – connect all pads together	Kelvin connect
VLO_FB	I	V1.5 feedback	
VLO_OUT	O	V1.5 output - connect all pads together	

### 1.2.2 Interface Pads

Table 1-2: Interface Pads

Pad Name	Type	Description				
RSTB	I	Asynchronous reset signal, L: reset				
SPB, MPU[1:0]	I	Interface mode selection signals				
		SPB	MPU1	MPU0	Interface Type	
		0	0	0	8-bit	68-mode (MIPI Type A)
			0	1	16-bit	68-mode (MIPI Type A)
			1	0	8-bit	80-mode (MIPI Type B)
			1	1	16-bit	80-mode (MIPI Type B)
		1	0	0	3/4-wire	SPI (9-bit) (MIPI Type C – option 1)
			0	1	3/4-wire	SPI (16-bit) (MIPI Type C – option 2)
			1	0	4/5-wire	SPI (8-bit) (MIPI Type C – option 3)
			1	1	3-wire 2-wire	SPI (8-bit) (1 byte start code) Serial (8-bit) (I <sup>2</sup> C compatible)
CSB	I	Chip select signal ( <b>all modes</b> ), L: enable interface, H: disable interface				
DCB	I	Interface access mode selection signal, L: Control; H: Data				
RWB_WRB_SPI	I	<b>68-mode:</b> Used as a Read/Write mode selection signal (L: Write, H: Read) <b>80-mode:</b> Used as a Write Pulse input (negative pulse) <b>SPI mode:</b> Must be tied high <b>I<sup>2</sup>C mode:</b> Must be tied low (low in conjunction with SPB, MPU[1:0] enables open drain function of SDA_SDO pad)				
E_RDB_SCL	I	<b>68-mode:</b> Used as a Enable Pulse input (positive pulse) <b>80-mode:</b> Used as a Read Pulse input (negative pulse) <b>SPI / I<sup>2</sup>C mode:</b> Serial data clock				

**Table 1-2: Interface Pads (continued)**

DB[17:16]	I	Unidirectional pads for data bits 17 to 16; RGB mode (DB[17] external clk In).
DB[15:0]	I/O	Bidirectional pads for data bits 15 to 0; RGB and parallel modes
SDI	I	<b>SPI mode:</b> Data in <b>I<sup>2</sup>C mode:</b> Not used
SDA_SDO	O	<b>SPI mode:</b> Data out <b>I<sup>2</sup>C mode:</b> Data in/out (open drain) – SYS_CLK / 64 output in test mode
TE	O	Tearing effect
VSYNC	I	V sync signal
HSYNC	I	H sync signal
PCLK	I	Dot-clock input
DE	I	RGB Data enable

### 1.2.3 OLED Driver Pads

**Table 1-3: OLED Driver Pads**

Pad Name	Type	Description
ANODEA<239:0>	O	OLED Anode driver outputs A (Red or Blue) (see Note 1)
ANODEB<239:0>	O	OLED Anode driver outputs B (Green)
ANODEC<239:0>	O	OLED Anode driver outputs C (Blue or Red) (see Note 1)
CATHODE<319:0>	O	OLED Cathode driver outputs

Note 1) In MADCTL(0x36) if Bit D3 = '0' ANODER represents the 'Red' component and ANODEB represents 'Blue'  
If D3 = '1' ANODER represents 'Blue' component and ANODEB represents 'RED' component

### 1.2.4 Other Pads

**Table 1-4: Miscellaneous Pads**

Pad Name	Type	Description
BRIGHT	I	Optical Sensor Input to ADC
BSTCTR	O	External VH booster control signal
EXTR	I	Display reference current, connect to ground via external resistor
DUMMY<7:0>	-	Dummy Pads (8 in total)

### 1.2.5 Test Pads

**Table 1-5: Test Pads**

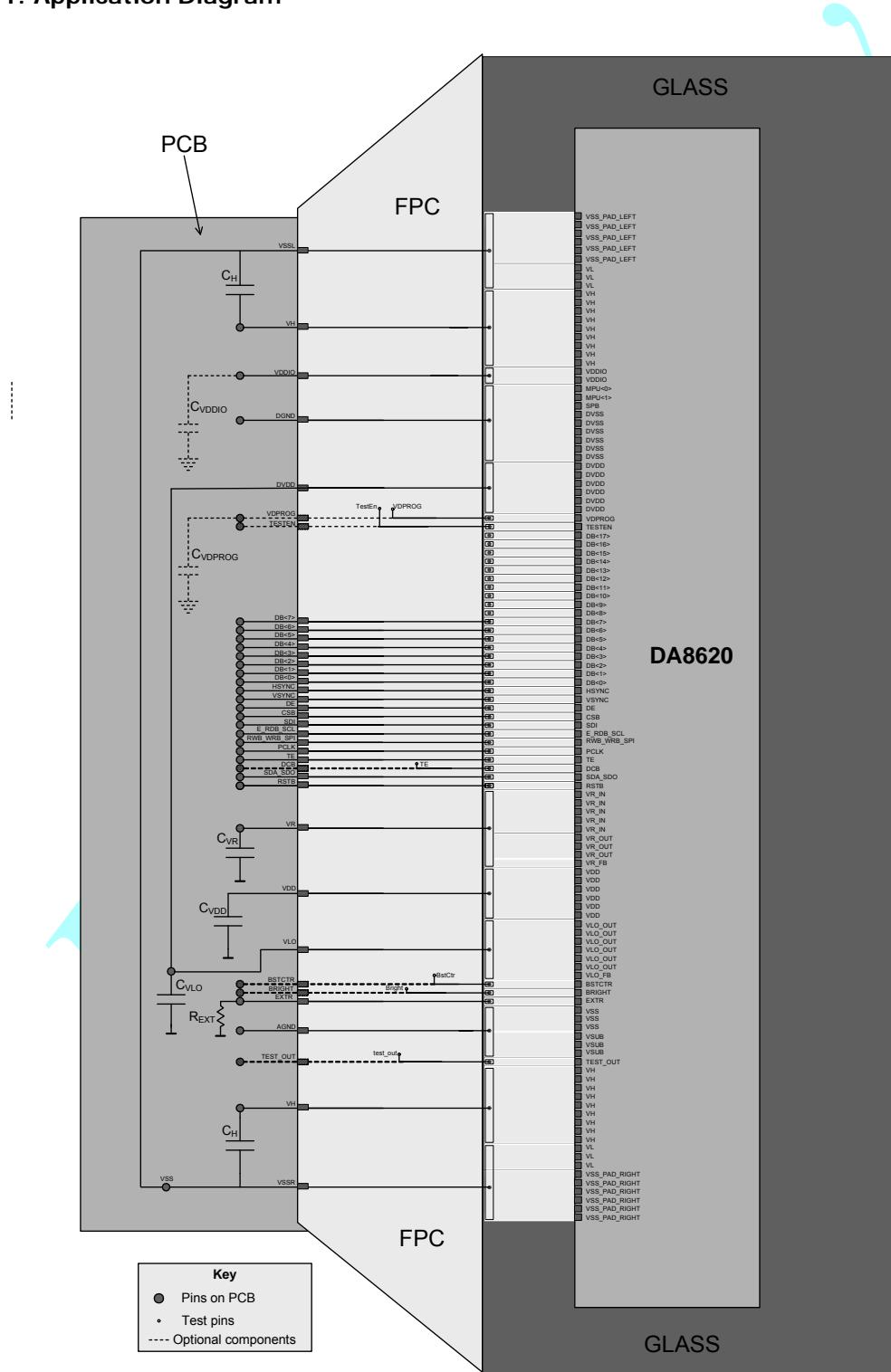
Pad Name	Type	Description
TESTEN		Test mode enable
TESTOUT		Test Out (Analogue test output pin)

## 2: Application and Orientation

## 2.1 Using the DA8620 in a practical product

Figure 2-1 shows an example showing how the DA8620 can be connected onto a module.

**Figure 2-1: Application Diagram**



Note that this arrangement allows the use of single sided flex. Components are shown on the PCB, but can alternatively be mounted on the FPC.

### 2.1.1 Discrete Component Values

**Table 2-1: Component values for typical application**

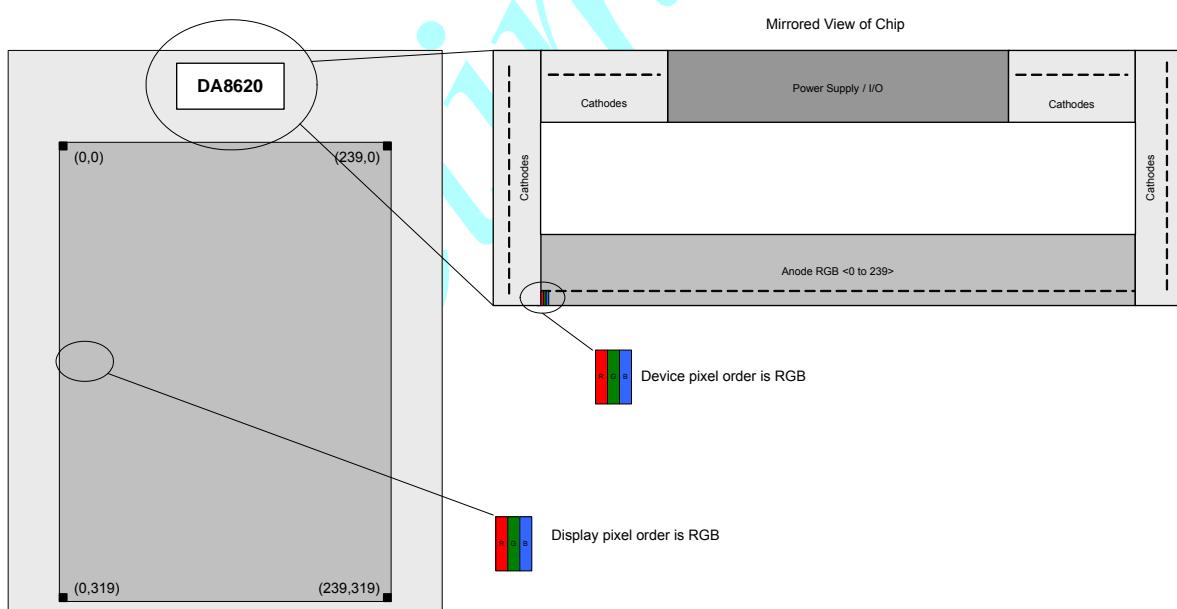
Component	Value (typical)	Voltage rating
C <sub>H</sub>	10 µF	32 V max
C <sub>VLO</sub>	10 µF	1.65 V max
C <sub>VR</sub>	10 µF	32 V max
C <sub>VDD</sub>	1 µF	5.5 V max
C <sub>VDPORG</sub>	1 µF	7.5 V max
C <sub>VDDIO</sub>	1 µF	5.5 V max
R <sub>EXT</sub>	56 kΩ	-

## 2.2 Orientation

### 2.2.1 Mounting Position

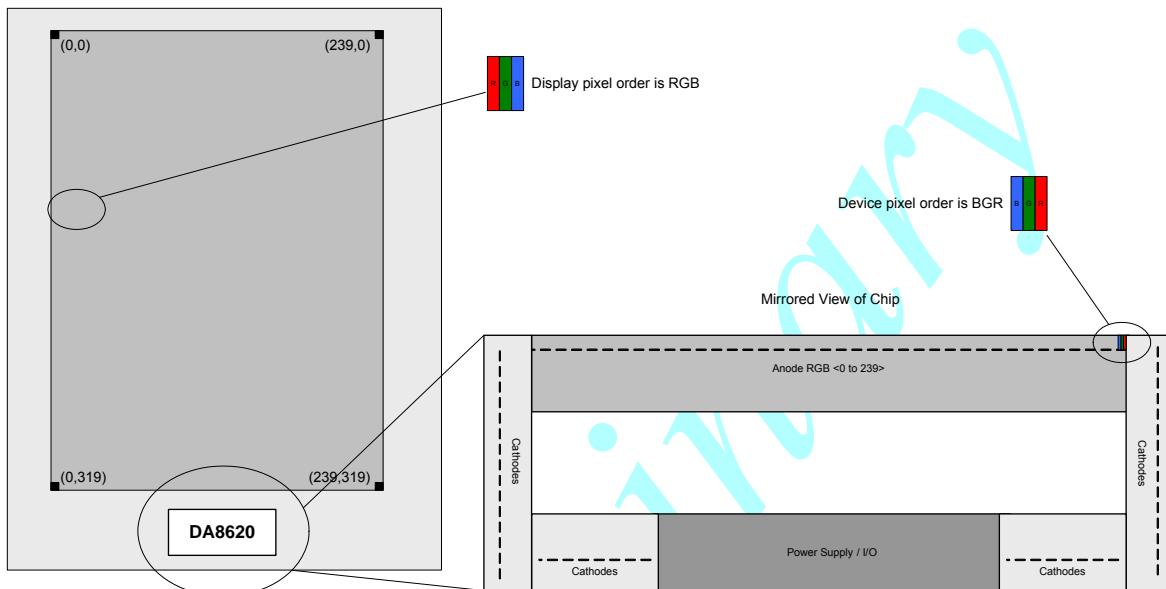
The default mounting position of the device is at the top of the glass as shown in Figure 2-2. The chip is shown mirrored to reflect the fact that it is flipped before being attached to the glass. This assumes the standard RGB pixel order.

**Figure 2-2: Top Mounted Device**



It is also possible to mount the device at the bottom of the display module as shown in Figure 2-3. In this orientation the (logically defined) cathodes and anodes no longer line up with their respective rows/columns. In this situation it is possible for the DA8620 to modify the order in which data is written into the RAM, in order to give the appearance of a normal display.

**Figure 2-3: Bottom Mounted Device**



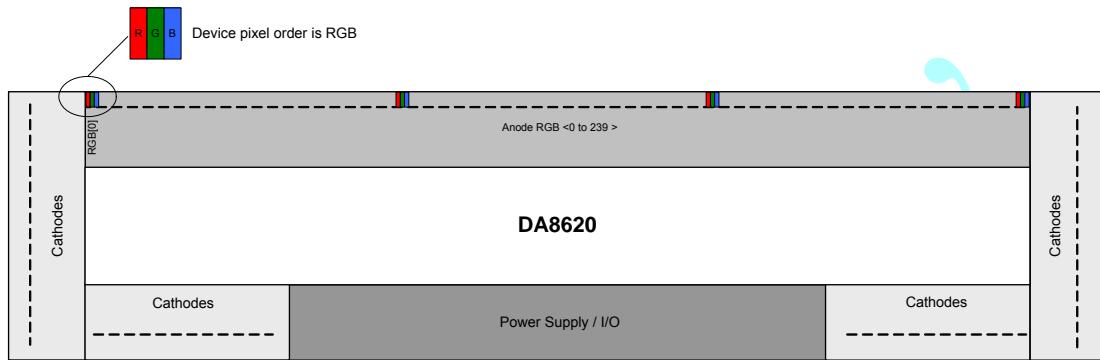
In order to produce a normal portrait display when the device is mounted at the bottom, it is necessary to make the bottom right RAM pixel appear as the top left display pixel and also to invert the order of the RGB, as the red anode will naturally align with the blue display pixel. To do this bits 7, 6 and 3 of the MADCTL (0x36) register could be set. However, instead of directly writing to the MADCTL (0x36) register the BM bit in the DCSCTL (0xC0) register can be used to invert the required signals so that a normal portrait display is produced. The BM bit will not affect the MADCTL register bits as seen by the host - it simply inverts bits 7, 6 and 3 as they leave the interface block and as they are then seen by the rest of the system. The Page Address and Column Address registers are not affected.

**Table 2-2: BM bit in the DCSCTL Register**

Address	OTP?	Name	Type	Bit values								Initial value						
				B7	B6	B5	B4	B3	B2	B1	B0							
0xC0	Yes	DCSCTL (DCS Control)	W	BW	BM	CS	CH	TE	SG	RGBOPT	MPUOPT	0x00						
				where:														
				BW	Black and White convert													
				BM	Bottom Mount device													
				CS	Clear Memory on SW Reset													
				CH	Clear Memory on HW Reset													
				TE	Output RSYNC on the TE pin													
				SG	A single Gamma Table													
				D1	RGBOPT for Pixel Format													
				D0	MPUOPT for Pixel Format													

The two diagrams above give a mirrored view of the chip because it is flipped before being attached to the glass. The natural view (gold bumps upwards) is shown below in Figure 2-4.

**Figure 2-4: Natural view of the DA8620 die**



## 3: DC Electrical Characteristics

### 3.1 Absolute Maximum Ratings

T<sub>a</sub> = 25°C, DVSS = VSS = 0 V

**Table 3-1: Driver Selection Characteristics**

Parameter	Symbol	Conditions	Min	Max	Units
Supply voltage - analog	VDD	VDD-DVSS	-0.3	5.5	V
Supply voltage - digital	DVDD	DVDD-DVSS	-0.3	1.65	V
Supply voltage - interface	VDDIO	VDDIO-DVSS	-0.3	5.5	V
Supply voltage - display	VH	VH - VSSDISPLAY	-0.3	32	V
Supply voltage - VR	VRIN	VRIN - VSSDISPLAY	-0.3	32	V
Input Voltage	VIN	All interface pads	-0.3	VDDIO + 0.3	V
Input Current	I <sub>i</sub>	I/O pads		-20	mA
Max. Output Current	I <sub>O</sub>	I/O pads		20	mA
Operating Ambient Temperature	T <sub>opr</sub>		-30	85	°C
Storage Ambient Temperature	T <sub>stg</sub>		-40	90	°C

**Warning:** The device quality may suffer if any absolute maximum rating parameter is exceeded, even momentarily. The absolute maximum ratings are values at which the device is on the verge of suffering physical damage. The device must be used below these conditions and precautions taken to ensure that the absolute maximum ratings are not exceeded.

### 3.2 Recommended Operating Conditions

T<sub>a</sub> = -30°C to +85°, DVSS = VSS = 0 V

**Table 3-2: Recommended Operating Conditions**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Supply Voltage	VDD	VDD-DVSS	2.4	2.8	5.0	V
	DVDD	DVDD-DVSS	1.425	1.5	1.575	V
	VDDIO	VDDIO-DVSS	1.6		5.0	V
	VH	VH - VSSDISPLAY	8.0	16.0	28.0	V
	VRIN	VRIN - VSSDISPLAY	3.0	13.0	28.0	V

### 3.3 DC Characteristics

T<sub>a</sub> = 27°C, VSS = DVSS = 0 V, VDD = 2.8 V DVDD = 1.5 V, VDDIO = 1.8 V, VH = 16 V, VRIN = 13 V

**Table 3-3: DC Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Input Leakage Current (high)	I <sub>IH1</sub>	Logic input pad VIH = DVDD			1	µA
Input Leakage Current (low)	I <sub>IL1</sub>	Logic input pad VIL = DVSS	-1			µA
Input High Level Voltage	VIH	Logic input pad	0.7 * VDDIO			V
Input Low Level Voltage	VIL	Logic input pad			0.3VDDIO	V
Output High Level Voltage	VOH1	Logic output pad IOH = -0.1 mA	VDDIO-0.2		VDDIO	V
Output Low Level Voltage	VOL1	Logic output pad IOL = 0.1 mA			0.2	V
Reference Current	I <sub>ref</sub>	I <sub>ref</sub> (Resistor = 56 kΩ)	TBD	10.7	TBD	µA

**Table 3-3: DC Characteristics (continued)**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
I DAC resolution RGB	IDACR,G,B	Iref		8		bit
I DAC values RGB	Dvair,G,B		0x00		0xFF	-
I DAC max. current: RGB	IAHR,G,B	Iref = 10 µA	- ½ LSB	133	+ ½ LSB	µA
I DAC min. current RGB	IALR,G,B			0		µA
I DAC diff. linearity	DLE R,G,B		-0.5		0.5	LSB
Precharge current DAC resolution	Dres2 R,G,B			8		bit
Precharge current DAC values	Dval2 R,G,B		0x00		0xFF	
Precharge DAC linearity	DLE R,G,B		-0.5		0.5	LSB
Precharge DAC min. current	IBL R,G,B	Iref = 10 µA		0		µA
Precharge DAC max. current		Iref = 10 µA	- ½ LSB	640	+ ½ LSB	µA
Precharge DAC diff.linearity error	DLE2 R,G,B		-½		+ ½	LSB
VR DAC resolution	Dres3			5		bit
VR DAC values	Dval3		0x00		0x1F	
VR DAC max.voltage	VDH3	This parameter is limited to Vh = 32 V		Vh		V
VR DAC min.voltage	VDL3		½ Vh - ½ LSB	½Vh	½ Vh + ½ LSB	V
VRDAC diff. linearity error	DLE3		-½		+½	LSB
Booster ctl DAC resolution	Dres4			8		bit
Booster ctl DAC values	DACval4		0x00		0xFF	
Booster ctl DAC max.current	IDH4		- 2%	25.6	+ 2%	µA
Booster ctl DAC min.current	IDL4			0		µA
IREF output impedance	Rlref				20	Ω

### 3.4 Driver Selection Characteristics

Ta = 27°C, VSS = DVSS = 0 V, VDD = 2.8V DVDD = 1.5 V, VDDIO = 1.8 V, VH = 16 V

**Table 3-4: Driver Selection Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Maximum output current (SLA)	IOH	ANODE R,G,B<239:0>	-133			µA
Output current deviation 1 (between two chips)	IOH1	ANODE R,G,B<239:0>: Vds (see Note 1) = 5.0 V (set to 100 µA)	TBD	3	TBD	%
Output current deviation 2 (within one chip)	IOH2	ANODE R,G,B<239:0>: Vds = 5.0 V (set to 100 µA) - after calibration	TBD	0.5	TBD	%
Current deviation 1 (between anodes)		Between adjacent output pads ANODE R,G,B<239:0> - after calibration	TBD	0.5	TBD	%
Anode current source head room	Vds	ANODE R,G,B<239:0>	1.5			V
Leakage current 1 when output is OFF	Ioff1	ANODE R,G,B<239:0>			TBD	µA
ON resistance between any anode and GND	RonAL1	ANODE R,G,B<239:0>: Vds = 2 V Vgs=18 V At room temp	TBD	500	TBD	Ω
ON resistance between any cathode and VRIN	RonKR1	CATHODE<319:0>: Vds = 2 V Vgs = 18 V, At room temp	TBD	200	TBD	Ω
ON resistance between any cathode and VSSDISPLAY	RonKL1	CATHODE<319:0>: Vds = 2 V Vgs=18 V At room temp	TBD	15	TBD	Ω

### 3.5 Handling

Inputs and outputs are protected against electrostatic discharge for normal handling. However, to be totally safe, normal CMOS handling precautions should be taken.

## 4: AC Characteristics

### 4.1 Clock Timing Characteristics

T<sub>a</sub> = -30°C to +85°C, DVSS = 0 V, VIN1 = DVDD = 2.2 to 3.3 V, VDDIO = 1.6 to 3.3 V

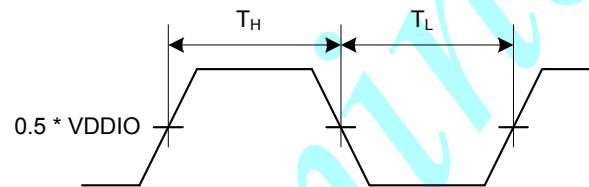
**Table 4-1: Clock Timing Characteristics**

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Internal RC oscillator frequency see Note 1)	F <sub>Int</sub>	T <sub>a</sub> = 25°C, VDD = 2.8 V	- 2%	10	+ 2%	MHz
Clock duty cycle (see Note 2))		Internal oscillator	35	50	65	%

Note 1) The internal oscillator frequency is not directly observable

Note 2) Duty Cycle (%) = TH / (TH + TL) × 100

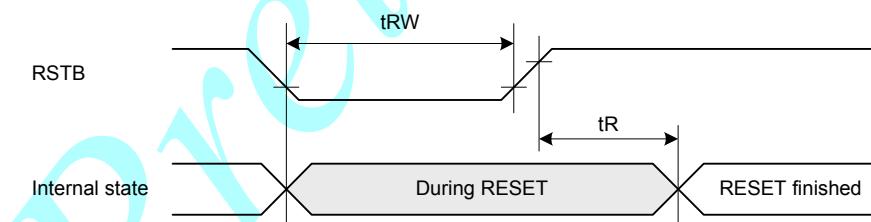
**Figure 4-1: Clock Waveform**



External clock is used for production testing and it is not recommended for normal operation.

### 4.2 Reset Timing Characteristics

**Figure 4-2: Reset timing**



**Table 4-2: Reset timing Characteristics**

Parameter	Symbol	Conditions	Min	Max	Units
Reset low pulse width	tRW		10 (TBC)		μs
Reset recovery time	tR		10 (see Note 1)		ms
			120 (see Note 2))		

Note 1) When Reset is applied during Sleep In Mode

Note 2) When Reset is applied during Sleep Out Mode.

It is necessary to wait 10 msec after releasing RSTB before sending commands.

Also the SLPOUT command cannot be sent for 120 msec.

#### Further notes:

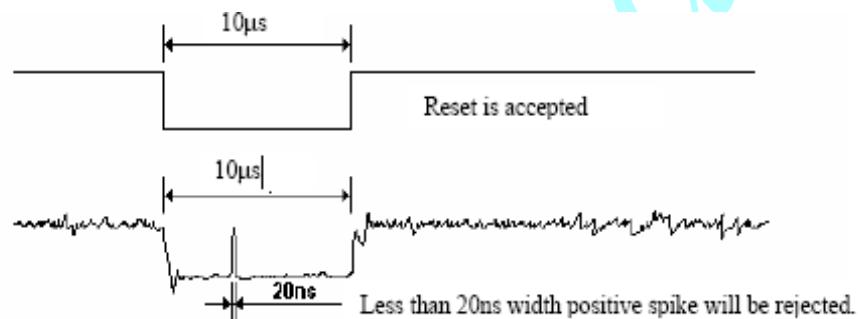
1. A hardware reset must be applied to the device when power is applied

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

**Table 4-3: Reset Action**

RSTB Pulse	Action
Shorter than 5µs	Reset Rejected
Longer than 9µs	Reset
Between 5µs and 9µs	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

**Figure 4-3: Reset Spike Rejection**

### 4.3 MIPI Type A – 68-mode Parallel Interface

Figure 4-4: 68-Mode Parallel Interface Timing

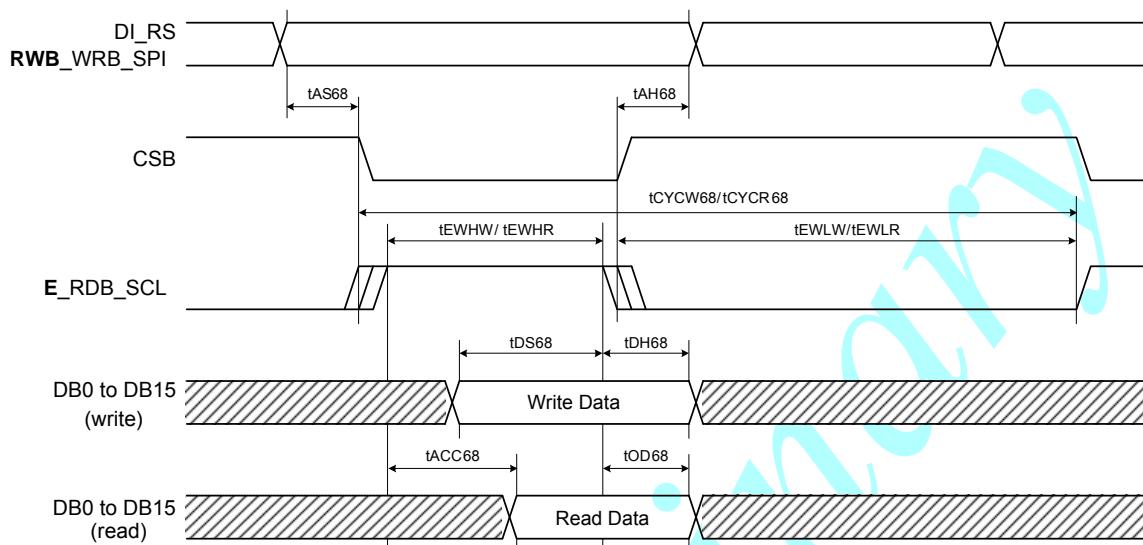


Table 4-4: 68-Mode Parallel Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Address Setup Time	tAS68		0			ns
Address Hold Time	tAH68		0			
Enable Width High Time	tEWHW	Write	30			
	tEWHR	Read	75			
Enable Width Low Time	tEWLW	Write	20			
	tEWLR	Read	75			
RAM Cycle Time	tCYCW68	Write	(see Note 1)			
	tCYCR68	Read				
Reg Cycle Time	tCYCW68	Write	50			
	tCYCR68	Read	150			
Data Setup Time	tDS68		10			
Data Hold Time	tDH68		20			
Read Access Time	tACC68	CL = 30pF			75	
Output Disable Time	tOD68	CL = 8pF	10			
		CL = 30pF			50	
Rising edge of all signals	tR	Low level = 30% of DVDD			15	
Falling edge of all signals	tF	High level = 70% of DVDD			15	

Note 1) System clock period dependent (see section 4.8)

#### 4.4 MIPI Type B – 80-mode Parallel Interface

Figure 4-5: 80-Mode Parallel Interface Timing

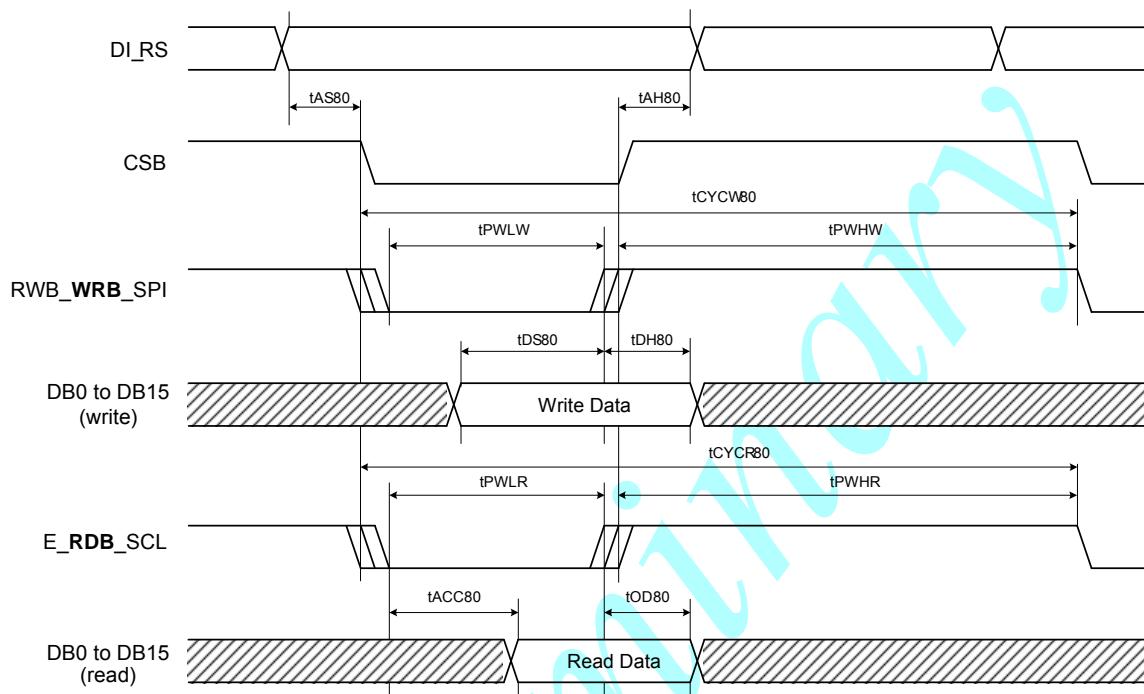


Table 4-5: 80-Mode Parallel Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Address Setup Time	tAS80		0			ns
Address Hold Time	tAH80		10			
Low Pulse Width	tPWLW	Write	25			
	tPWLR	Read	75			
High Pulse Width	tPWHW	Write	15			
	tPWHR	Read	75			
RAM Cycle Time	tCYCW80	Write	(see Note 1)			
	tCYCR80	Read				
Reg Cycle Time	tCYCW68	Write	40			
	tCYCR68	Read	150			
Data Setup Time	tDS80		20			
Data Hold Time	tDH80		10			
Read Access Time	tACC80	CL = 30 pF			75	
Output Disable Time	tOD80	CL = 8 pF	20			
		CL = 30 pF			80	
Rising edge of all signals	tR	Low level = 30% of DVDD			15	
Falling edge of all signals	tF	High level = 70% of DVDD			15	

Note 1) System clock period dependent. See section 4.8.

## 4.5 MIPI Type C – Serial Peripheral Interface

Figure 4-6: MIPI Type C Interface Timing

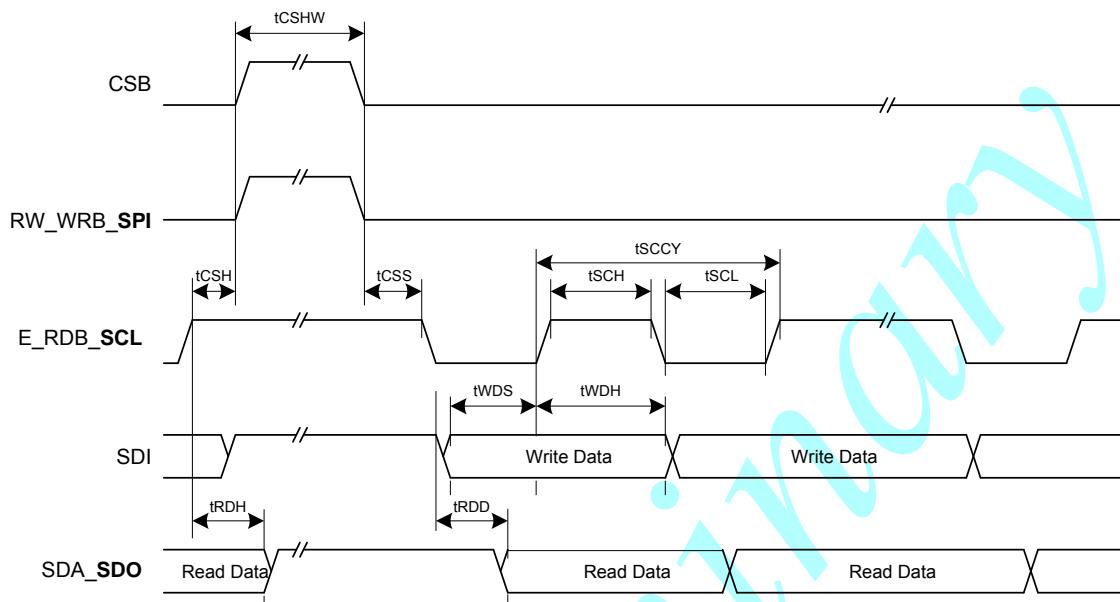
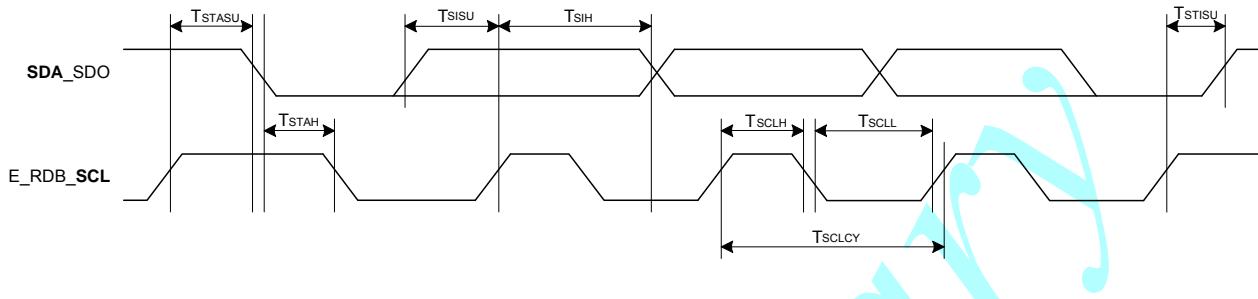


Table 4-6: MIPI Type C Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCL cycle time	tSCCY	Write	100			ns
		Read	180			
SCL low time	tSCL	Write	50			
		Read	90			
SCL high time	tSCH	Write	50			
		Read	90			
CSB setup time	tCSS		10			
CSB hold time	tCSH		50			
CSB high level width	tCSHW		100			
Write data setup time	tWDS		10			
Write data hold time	tWDH		40			
Read data delay	tRDD	For min time CL=8 pF	40			
		For max time CL=30 pF			80	

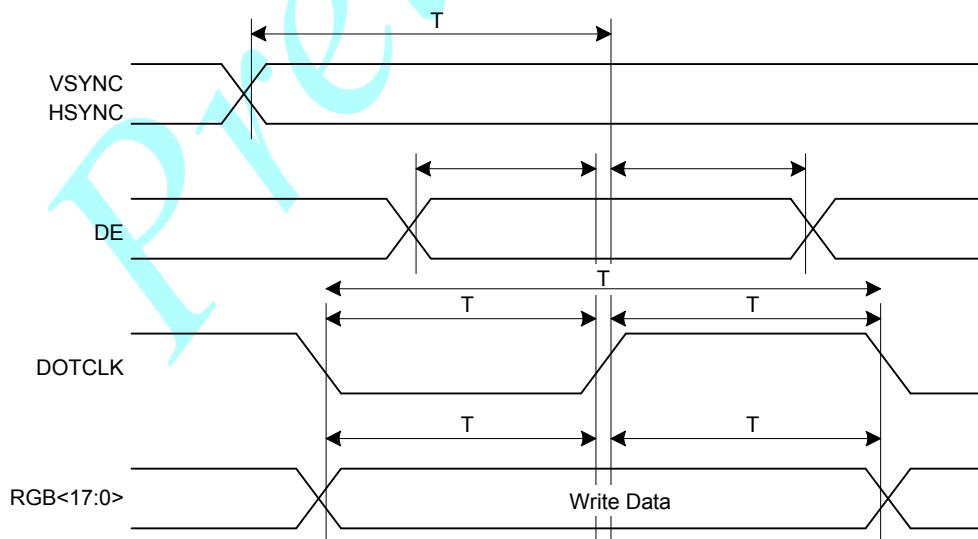
## 4.6 I<sup>2</sup>C Interface

Figure 4-7: I<sup>2</sup>C Interface TimingTable 4-7: I<sup>2</sup>C Interface Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Clock frequency	F <sub>SCL</sub>	V <sub>DIO</sub> = 2.8 V. All signal timing is based on 20% to 80% V <sub>DIO</sub> and a maximum rise and fall time of 10 ns			400	KHz
SCL cycle time	T <sub>SCLCY</sub>		2.5			μs
SCL high time	T <sub>SCLH</sub>		600			ns
SCL low time	T <sub>SCLL</sub>		1.3			μs
SCL start set-up time	T <sub>STASU</sub>		600			
SCL start hold time	T <sub>STAH</sub>		600			
SI data set-up time	T <sub>TSISU</sub>		100			ns
SI data hold time	T <sub>SIH</sub>		100			
SCL stop set-up time	T <sub>STOSU</sub>		600			

## 4.7 RGB Interface

Figure 4-8: RGB Interface timing



**Table 4-8: RGB Interface characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Dot Clock frequency	PCLK				(see Note 1)	MHz
Dot Clock high time			20			ns
Dot Clock low time			20			ns

Note 1) System clock period dependent. See section 5.8.

## 4.8 Interface Clock Period

The interface clock period is dependent upon system clock period.

The table below contains the possible maximum interface cycle times for various pixel formats and interface widths.

**Table 4-9: Maximum Interface Clock Rate vs Interface Width / Pixel Format**

Pixel Format	Option (see Note 1)	Interface				Units
		18-bit	16-bit	9-bit	8-bit	
24 bpp	option 1	260	130	---	105	ns
	option 2	105	130	---	---	
18 bpp	option 1	260	130	130	---	ns
	option 2	105	130	130	---	
16 bpp	option 1	260	260	---	130	ns
	option 2	130	---	---	130	
12 bpp	option 1	260	260	---	130	ns
	option 2	130	---	---	---	
8bpp	option 1	520	520	---	260	ns
	option 2	260	---	---	---	

Note 1) For definition of options, see section 6.2.3.2

Example: If a 16-bit bus MPU interface is used with a 24 bits-per-pixel format, the write cycle time of the parallel interface will be 130 ns.

## 5: MPU Interface

### 5.1 Introduction

The DA8620 supports two different styles of interface: (i) a bidirectional MPU interface which is used to access the control registers or the display RAM; and (ii) an RGB interface which is unidirectional and can only send data to the display RAM. Both interfaces share the data bus DB[15:0].

If the MPU interface needs to support video data then one of the parallel interface styles should be used, as the bandwidth of the serial interfaces is restrictive.

Specifically, DA8620 supports the MIPI DBI Type A and B parallel interfaces: these are compatible with the industry standard m68 and i80 interfaces respectively. It also supports all three versions of the MIPI DBI Type C serial interface (, along with generic 2- and 3-wire interfaces which are compatible with industry standard SPI and I<sup>2</sup>C peripherals and a 4/5 wire serial interface.

The RGB-style interface complies with the MIPI DPI specification.

The serial MPU interface can be used at the same time as the RGB interface and, although capable of accessing the display RAM, it is expected to be used to access the register-based command set only.

The SPB pad (Serial/Parallel) is used to select between RGB / serial MPU and the parallel MPU modes.

**Table 5-1: The Serial/Parallel Mode Selection Pad**

SPB	Interface mode
0	68-mode (MIPI Type A) 80-mode (MIPI Type B)
1	2/3/4 wire serial 18-bit RGB

### 5.2 MPU Interface Mode Selection

The MPU interface is selected via the SPB and MPU[1:0] pads. These can be hard-wired on the display module or connected to GPIO for maximum flexibility. Whenever one of the serial interfaces is selected, the DB[17:0] pads are made available for use by the RGB interface.

The MPU interface can be used to access all control registers and the display RAM. All control registers have default to read, write, or control as specified by the MIPI DCS specification. In addition the MPU interface can also use the RW signal (available as either a control bit or a separate pin) to override the default action, allowing registers that are normally write-only to be read.

A special test mode is available to enable all registers to be read, even if the serial interface does not support the RW signal or control bit. Table 5-2 shows the settings for interface mode selection:

**Table 5-2: Interface mode selection**

SPB	MPU[1]	MPU[0]	Interface mode
0	0	0	8-bit 68-mode (MIPI Type A)
	0	1	16-bit 68-mode (MIPI Type A)
	1	0	8-bit 80-mode (MIPI Type B)
	1	1	16-bit 80-mode (MIPI Type B)
1	0	0	3/4-wire SPI (9-bit) (MIPI Type C – option 1)
	0	1	3/4-wire SPI (16-bit) (MIPI Type C – option 2)
	1	0	4/5-wire SPI (8-bit) (MIPI Type C – option 3)
	1	1	3-wire SPI (8-bit) (1-byte start code)
			2-wire serial (8-bit) (I <sup>2</sup> C compatible)

Notes:

1. RWB\_WRB\_SPI pin defines the functionality of SDA\_SDO pin in the 3-wire SPI mode and I<sup>2</sup>C modes.

#### 2. Break and Pause of Sequences.

According to the MIPI DBI spec (7.3.3), the host processor can break a read or write sequence by pulling the CSB signal high during a command or data byte (intra-byte). The display module shall reset its interface so it will be ready to receive the same byte when CSB is again driven low.

The host processor can pause a read or write sequence by pulling the CSB signal high between command or data bytes (inter byte). The display module shall wait for the host processor to drive CSB low before continuing the read or write sequence at the point where the sequence was paused.

### 5.3 MIPI Type A - 68-mode

The type A interface supports two modes: Fixed E and Clocked E (**E\_RDB\_SCL** pin). Both modes utilize the CSB, DCB, **RWB\_WRD\_SPI** and **E\_RDB\_SCL** signals as well as eight (DB[7:0]), nine (DB[8:0]) or sixteen (DB[15:0]) data lines.

DCB is driven low while a command is present on the interface and pulled high when data is on the interface.

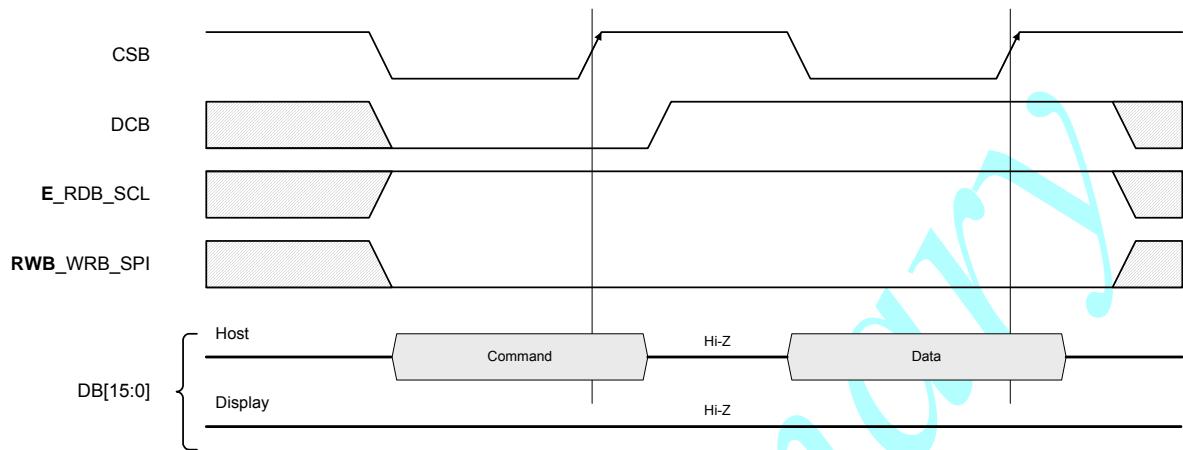
The TE signal is optional and can be used to indicate the current display position within the frame for synchronization purposes. Table 5-3 below summarizes all the relevant signals:

**Table 5-3: 68-Mode Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset (active low)
CSB	I	Chip Select. In Fixed E mode, the host processor writes data on the falling edge of CSB, or reads on the rising edge. In Clocked E mode, the DA8620 is selected when CSB is low.
DCB	I	Data / Command Select. Data is indicated when high and Command is indicated when low.
<b>RWB_WRB_SPI</b>	I	Read / Write. Host processor reads data when RWB is high or writes data when RWB is low.
<b>E_RDB_SCL</b>	I	Clock. In Fixed E mode, this signal is tied high. In Clocked E mode, the host processor reads data on the rising edge of E, or writes on the falling edge.
TE	O	Tearing Effect (optional)
SDI	I	Serial Data In is not used and can be left unconnected.
SDA_SDO	O	Serial Data Out is not used and can be left unconnected.
SPB	I	Must be set to 0 to select parallel interface mode
MPU[1:0]	I	Must be set to 0x0 (binary 00) for 8-bit interface and 0x1 (binary 01) for 16-bit.

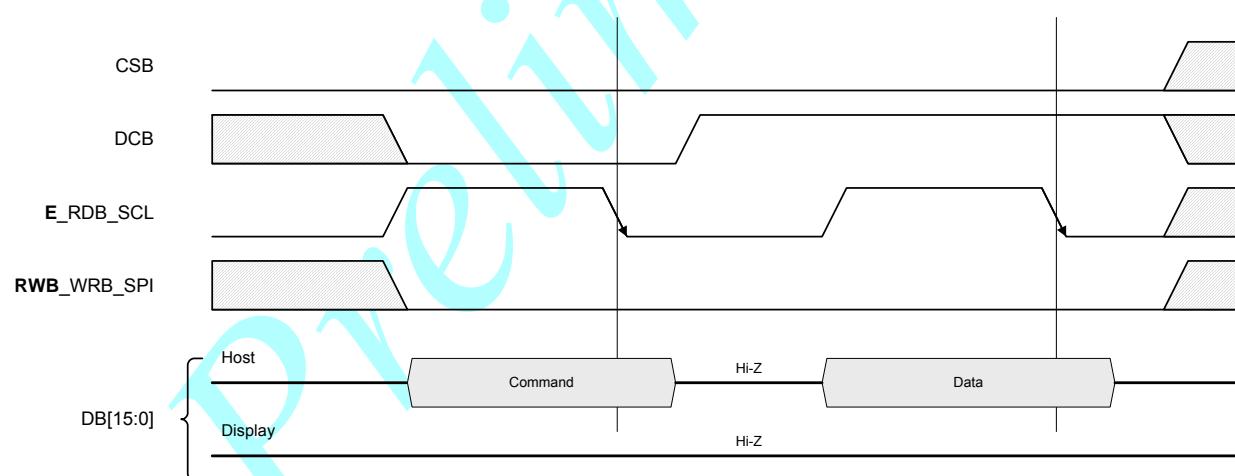
The two basic 68-mode write cycle timing diagrams are shown in the following two figures:

Figure 5-1: 68-Mode Fixed E-mode Write Sequence



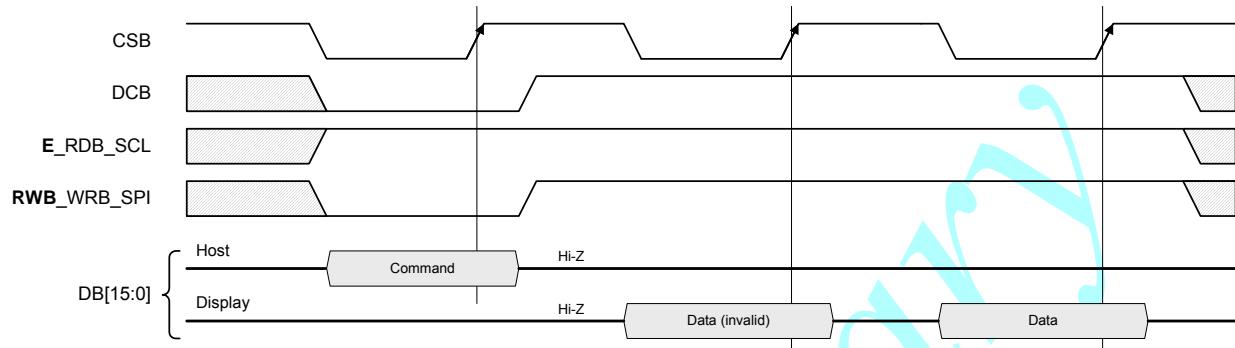
Notes: (i) The host writes the command / data on the falling edge of CSB.  
(ii) The display latches the command / data on the rising edge of CSB.

Figure 5-2: 68-Mode Clocked E-mode Write Sequence



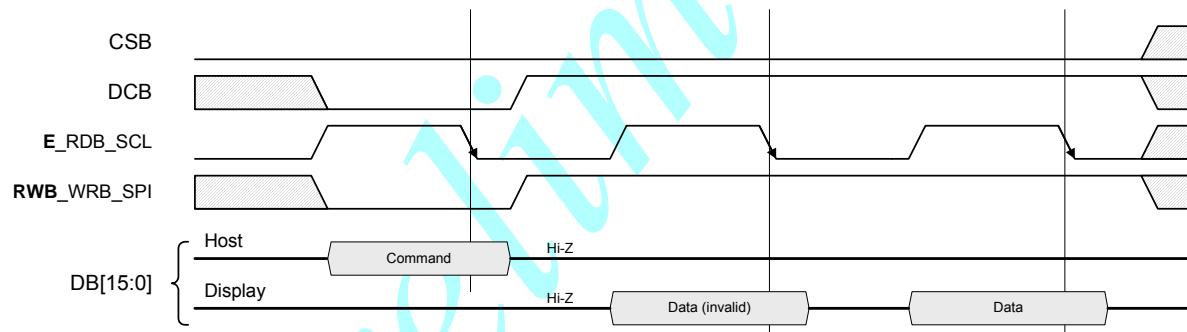
Notes: (i) The host writes the command / data on the rising edge of E  
(ii) The display latches the command / data on the falling edge of E

Figure 5-3: 68-Mode Fixed E-mode Read Sequence



Notes: (i) The host writes the command on the falling edge of CSB and latches the data on the rising edge  
(ii) The display latches the command on the rising edge of CSB and writes the data on the falling edge

Figure 5-4: 68-Mode Clocked E-mode Read Sequence



Notes: (i) The host writes the command on the rising edge of E and latches the data on the falling edge  
(ii) The display latches the command on the falling edge of E and writes the data on the rising edge

## 5.4 MIPI Type B - 80-mode

The Type B interface utilizes DCB, E\_RDB\_SCL and RWB\_WRB\_SPI signals as well as eight (DB[7:0]), nine (DB[8:0]) or sixteen (DB[15:0]) data lines. RWB\_WRB\_SPI is driven from high to low then pulled back to high during the write cycle. DCB is driven low while command information is on the interface and is pulled high when data is present.

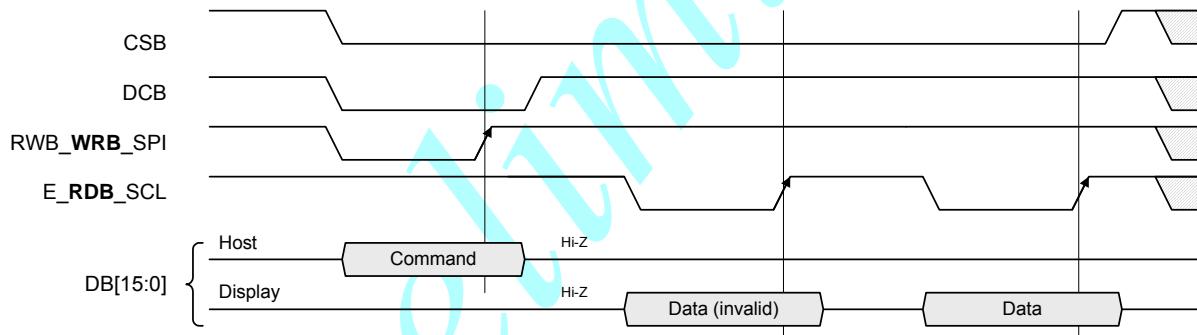
**Table 5-4: 80-Mode Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset (active low)
CSB	I	Chip Select. The DA8620 is selected when CSB is low.
DCB	I	Data / Command Select. Data is indicated when high and Command is indicated when low.
RWB_WRB_SPI	I	Write. Host processor writes data on the falling edge of WRB.
E_RDB_SCL	I	Read. Host processor reads data on the rising edge of RDB.
TE	O	Tearing Effect (optional)
SDI	I	Serial Data In is not used and can be left unconnected.
SDA_SDO	O	Serial Data Out is not used and can be left unconnected.
SPB	I	Must be set to 0 to select parallel interface mode
MPU[1:0]	I	Must be set to 0x2 (binary 10) for 8-bit interface and 0x3 (binary 11) for 16-bit.

The basic read and write timing diagrams are shown below in Figure 5-5 and Figure 5-6.

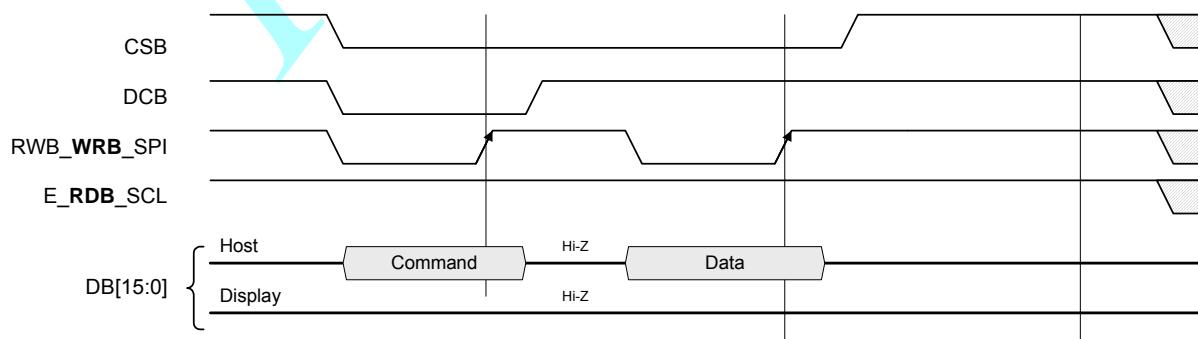
Note: This mode supports paused commands when CSB is removed between transactions.

**Figure 5-5: 80-Mode Read Sequence**



Notes: (i) The host writes the command on the falling edge of WRB and latches the data on the rising edge of RDB  
(ii) The display latches the command on the rising edge of WRB and writes the data on the falling edge of RDB

**Figure 5-6: 80-Mode Write Sequence**



Notes: (i) The host writes the command / data on the falling edge of WRB  
(ii) The display latches the command / data on the rising edge of WRB

## 5.5 MIPI Type C - 9-bit SPI (Option 1)

MIPI Type C (option 1) is a 3/4-wire 9-bit serial interface. The chip-select CSB (active low) enables and disables the serial interface. RSTB (active low) is an external reset signal. E\_RDB\_SCL is the serial data clock and SDA\_SDO is the serial data. The interface can also operate as a 4-wire SPI with separate data in (SDI) and out (SDA\_SDO). When operated in a 3-wire mode the SDA\_SDO pad should be connected to the SDI pad.

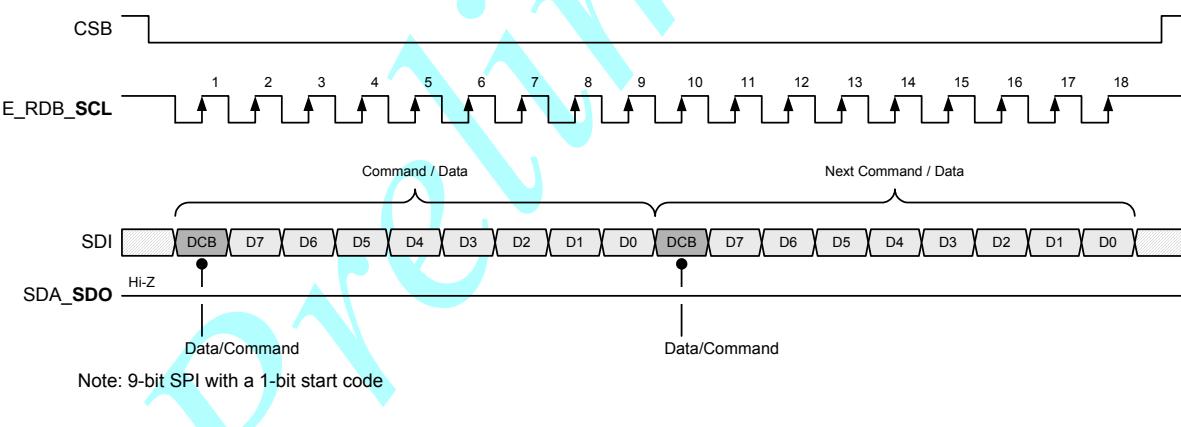
SCL is not a continuous clock and it can be stopped by the MCU when SCL signal is low or high. SCL and SDI / SDO\_SDA can be high or low when there is a falling or rising edge of the CSB signal.

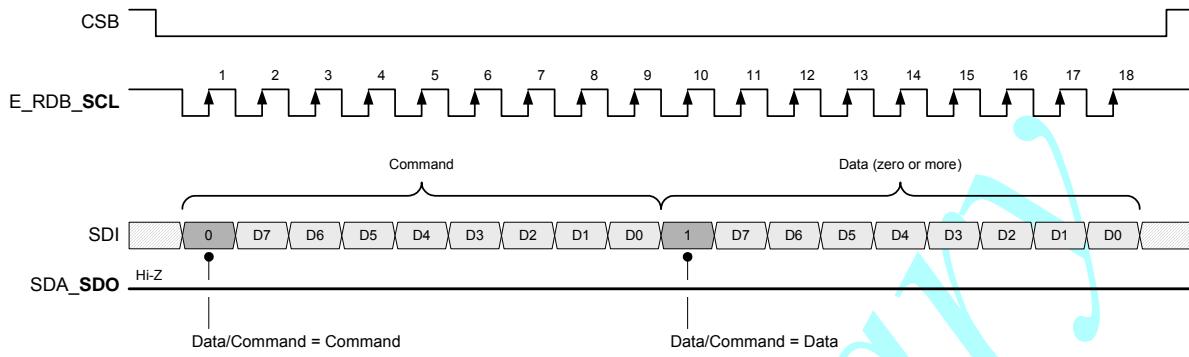
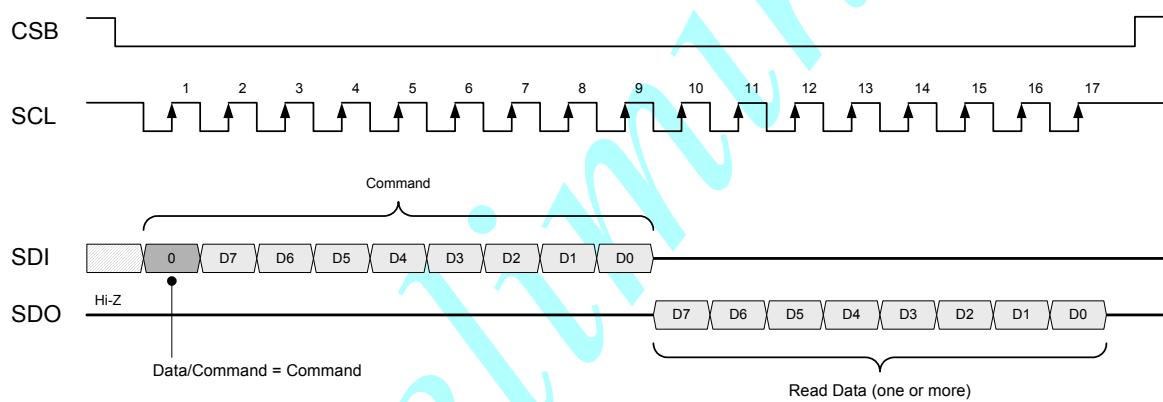
**Table 5-5: 9-bit SPI (Option 1) Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset
CSB	I	Chip Select
DCB	I	Data / Command Select is not used and can be left unconnected
RWB_WRB_SPI	I	Must be set to 1 to select SPI mode
E_RDB_SCL	I	Serial Clock
SDI	I	Serial Data In
SDA_SDO	O	Serial Data Out (open drain)
SPB	I	Must be set to 1 to select serial interface mode
MPU[1:0]	I	Must be set to 0x0 (binary 00) to select MIPI Type C – opt 1

Serial data must be input to SDI in the sequence DCB, D7 to D0. The DA8620 reads the data at the rising edge of the SCL signal. The first bit of serial data DCB is data/command flag. When DCB = "1", D7 to D0 bits are display RAM data or command parameters. When DCB = "0" D7 to D0 bits are commands.

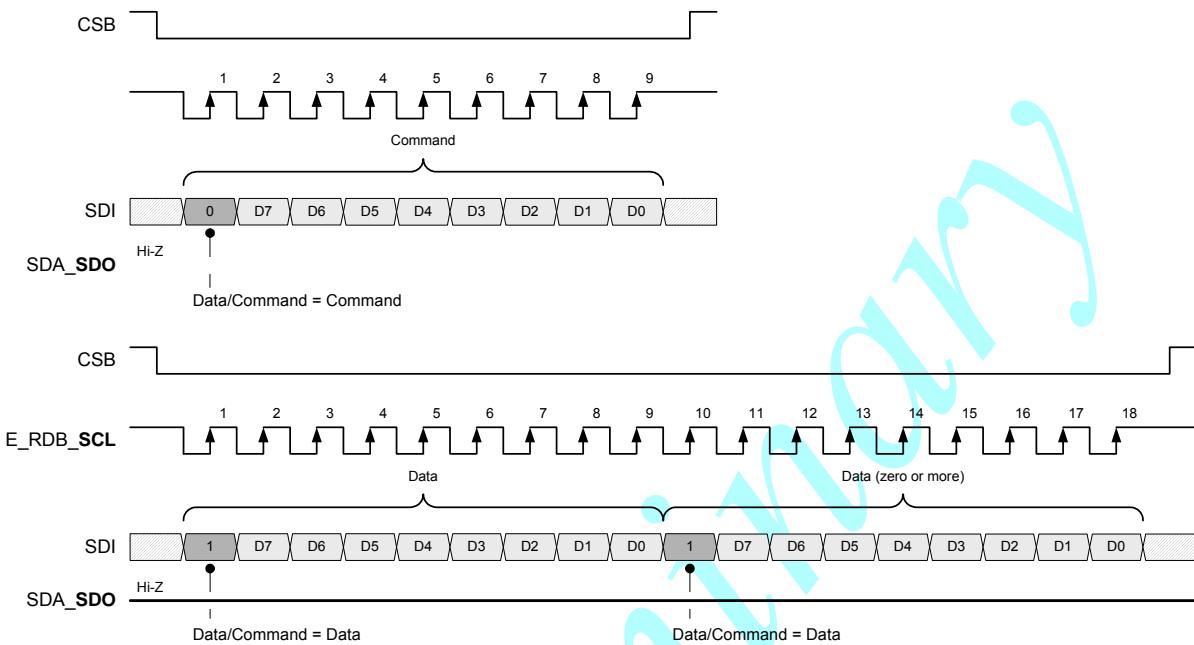
**Figure 5-7: MIPI Type C (Option 1) Generic Command Format**



**Figure 5-8: MIPI Type C (Option 1) Write Command with Parameters****Figure 5-9: MIPI Type C (Option 1) Read Command with Parameters****Notes:**

1. It is possible to pause a write command by taking CSB high between command and parameter or between parameters.

2. A read command cannot be paused as the rising edge of CSB terminates the command.

**Figure 5-10: MIPI Type C (Option 1) Paused Write Command**

Note: If the command corresponds to a read-only address (or has no parameters) then the data is ignored

## 5.6 MIPI Type C - 16-bit SPI (Option 2)

MIPI Type C (option 2) is a 3/4-wire 16-bit serial interface. The chip-select signal CSB (active low) enables and disables the serial interface. RSTB (active low) is an external reset signal. E\_RDB\_SCL is the serial data clock and SDA\_SDO is the serial data output. The interface can also operate as a 4-wire SPI with separate data in (SDI) and out (SDA\_SDO). When operated in a 3-wire mode the SDA\_SDO pad should be connected to the SDI pad.

**Table 5-6: 16-bit SPI (Option 2) Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset
CSB	I	Chip Select
DCB	I	Data / Command Select is not used and can be left unconnected
RWB_WRB_SPI	I	Must be set to 1 to select SPI mode
E_RDB_SCL	I	Serial Clock
SDI	I	Serial Data In
SDA_SDO	O	Serial Data Out (open drain)
SPB	I	Must be set to 1 to select serial interface mode
MPU[1:0]	I	Must be set to 0x1 (binary 01) to select MIPI Type C – opt 2

As with the MIPI Type C (option 1) interface, the read data is 8-bits (not the 16-bits). This has the same implications concerning pauses and breaks as described in the section on option 1 (Section 5.5 above).

**Figure 5-11: MIPI Type C (Option 2) Generic Read Command**

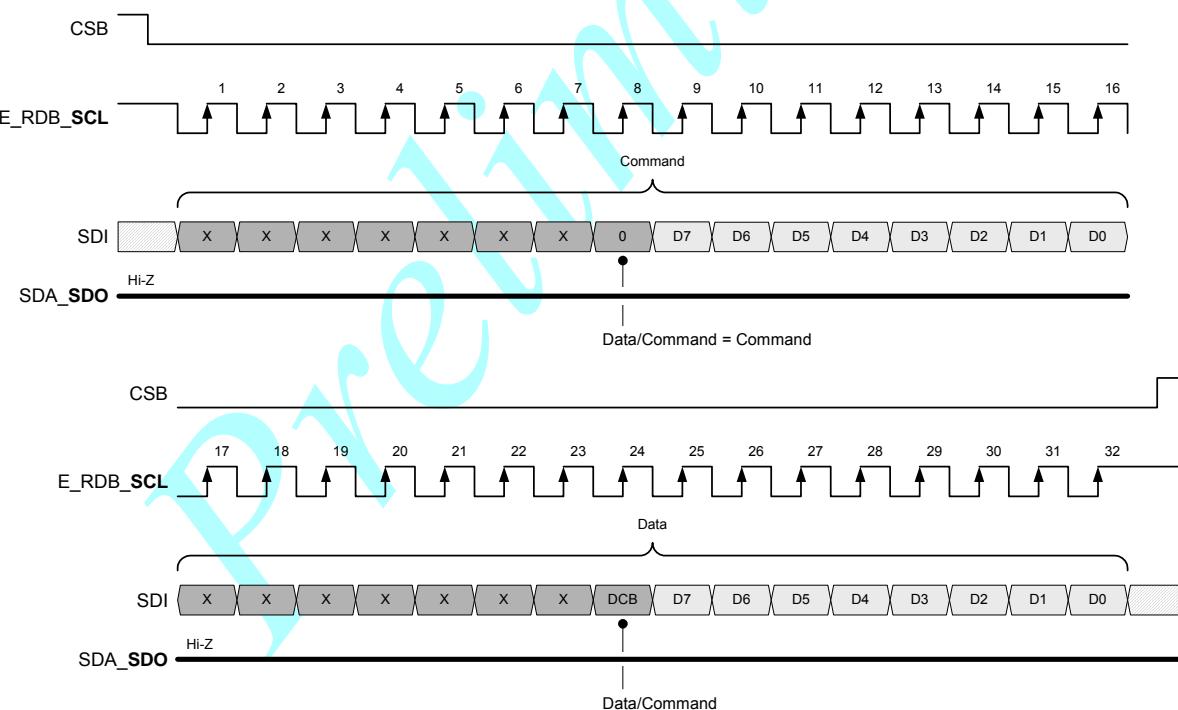


Figure 5-12: MIPI Type C (Option 2) Write Command with Parameters

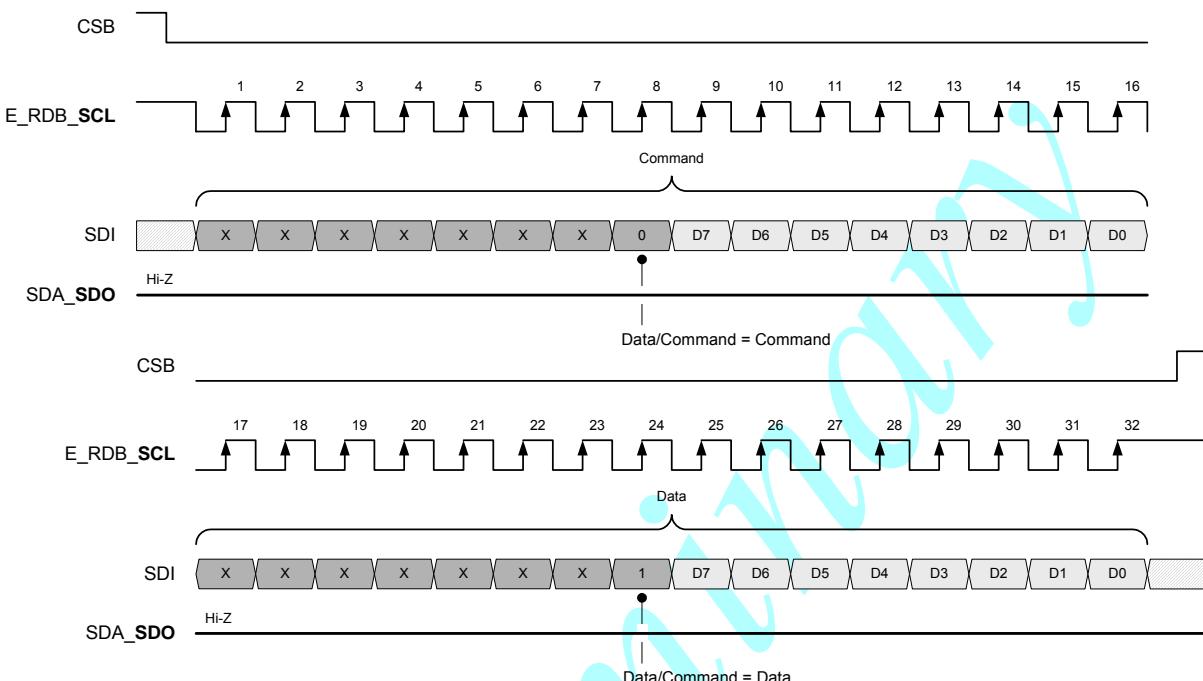
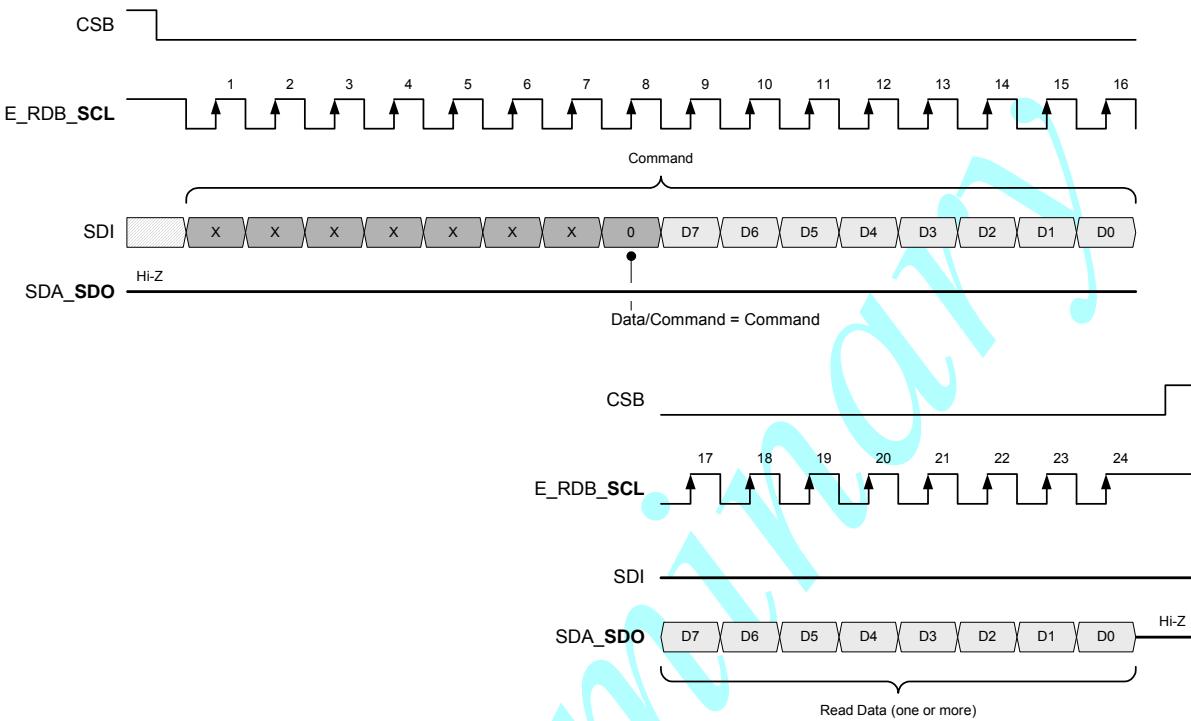


Figure 5-13: MIPI Type C (Option 2) Read Command with Parameters



Note: (i) If the command corresponds to a write-only address then the dummy data is ignored and the current register contents are returned as read data.  
(ii) A read command is always terminated with a rising edge on CSB (from Nokia spec DMIF-S31BL-A01).  
(iii) A paused read command does not exist.

## 5.7 MIPI Type C - 8-bit SPI (Option 3)

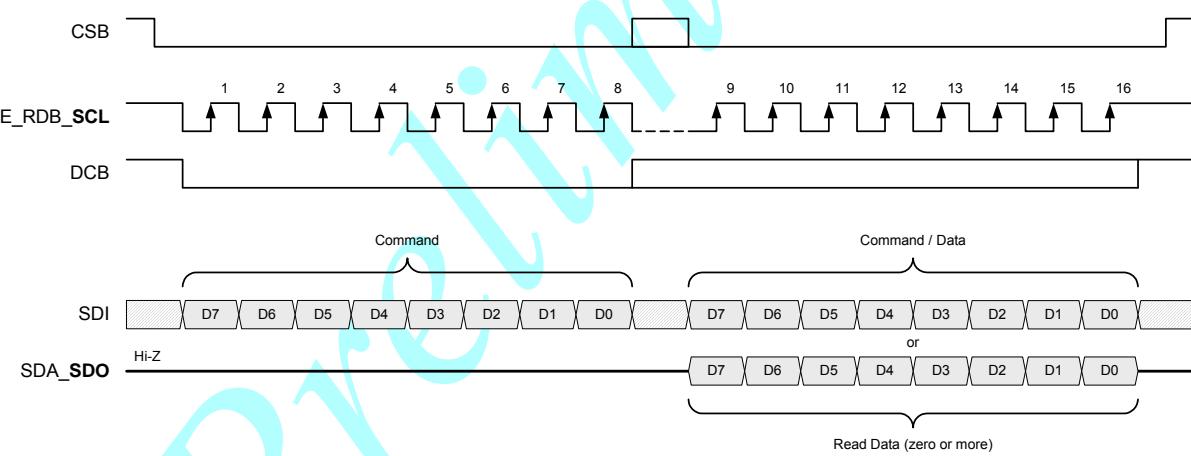
MIPI Type C (option 3) is a 4/5-wire 8-bit serial interface. The chip-select CSB (active low) enables and disables the serial interface. RSTB (active low) is an external reset signal. E\_RDB\_SCL is the serial data clock, SDA\_SDO is the serial data, and the DCB signal is used to distinguish commands (active low) from data (active high). The interface can also operate as a 5-wire SPI with separate data in (SDI) and out (SDA\_SDO). When operated in a 4-wire mode the SDA\_SDO pad should be connected to the SDI pad.

**Table 5-7: 8-bit SPI (Option 3) Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset
CSB	I	Chip Select
DCB	I	Data / Command Select
RWB_WRB_SPI	I	Must be set to 1 to select SPI mode
E_RDB_SCL	I	Serial Clock
SDI	I	Serial Data In
SDA_SDO	O	Serial Data Out (open drain)
SPB	I	Must be set to 1 to select serial interface mode
MPU[1:0]	I	Must be set to 0x2 (binary 10) to select MIPI Type C – opt 3

The generic command format is given below. This interface has a uniform byte length of 8-cycles and supports pause and break for write commands.

**Figure 5-14: MIPI Type C (Option 3) Generic Command**



Note: A Pause Read command does not exist.

## 5.8 Dialog 3-wire SPI

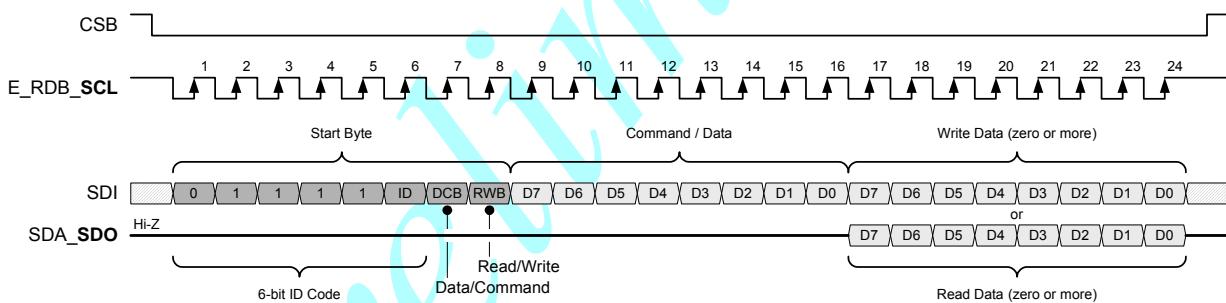
All commands and data are 8-bits. Multiple commands per transfer are not allowed. Every transfer starts with an 8-bit start code. Taking CSB high before a byte has completed will abort the transfer - the next byte must then match the 6-bit ID code before it is considered valid. The interface can also operate as a 4-wire SPI with separate data in (SDI) and out (SDA\_SDO). When operated in a 3-wire mode the SDA\_SDO pad should be connected to the SDI pad.

**Table 5-8: Dialog 3-wire SPI Signals**

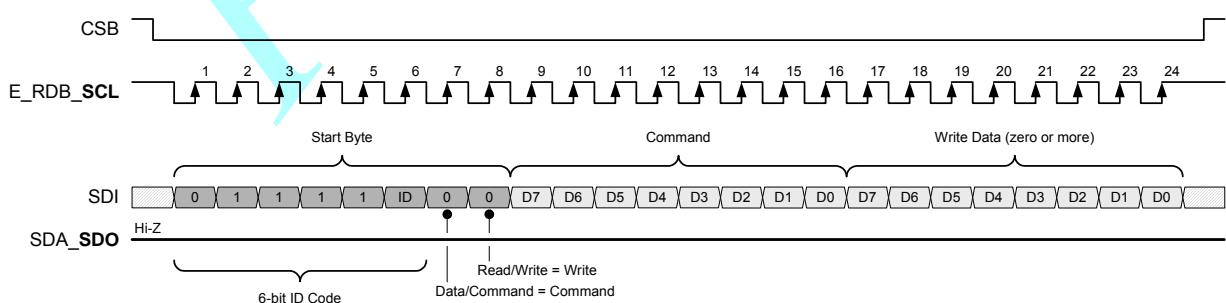
Pad Name	Type	Description
RSTB	I	Asynchronous Reset
CSB	I	Chip Select
DCB	I	Data / Command Select is not used and can be left unconnected
RWB_WRB_SPI	I	Must be set to 1 to select SPI mode
E_RDB_SCL	I	Serial Clock
SDI	I	Serial Data In
SDA_SDO	O	Serial Data Out (open drain)
SPB	I	Must be set to 1 to select serial interface mode
MPU[1:0]	I	Must be set to 0x3 (binary 11) to select Dialog SPI

The generic command format is shown below in Figure 5-15. This interface has a uniform byte length of 8-cycles and supports pause and break for both read and write commands. As with the MIPI SPI write modes, the Dialog SPI mode requires the start code to be re-sent at the start of every transfer, even when the subsequent transfer is a continuation (following a pause) of the first.

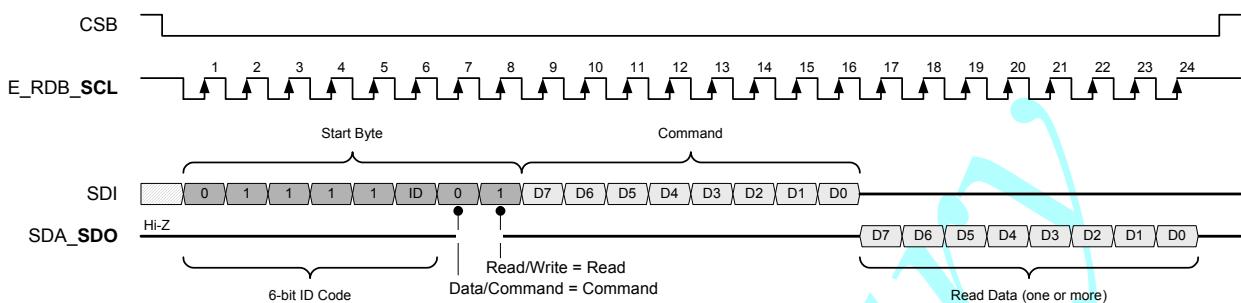
**Figure 5-15: Dialog SPI Generic Command**



**Figure 5-16: Dialog SPI Write Command with parameters**



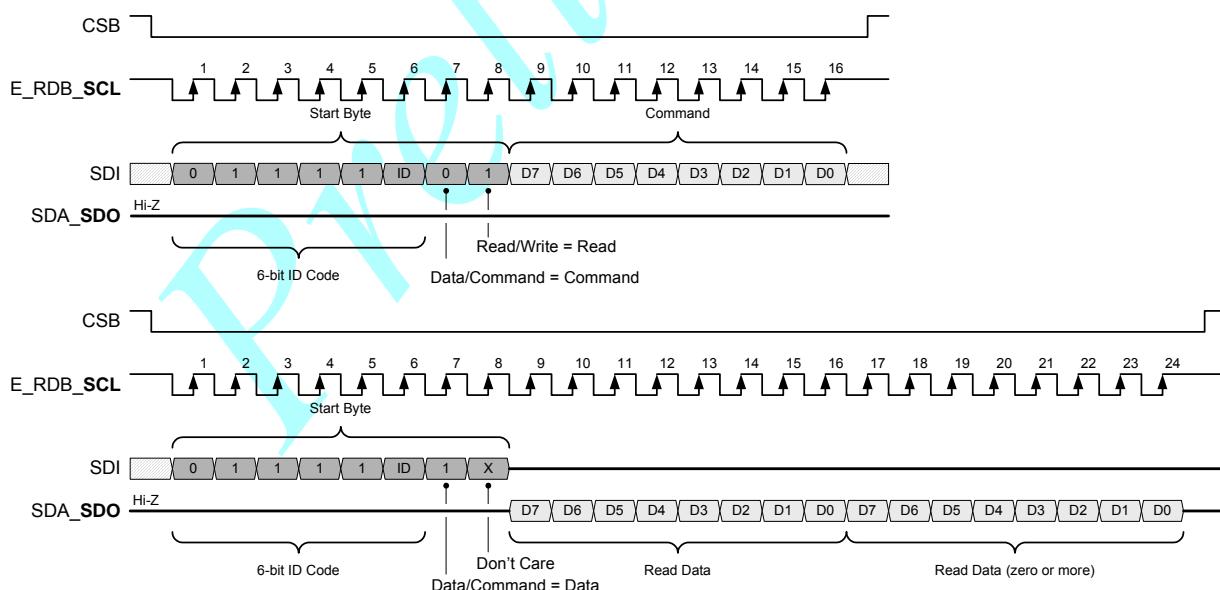
Note: If the command corresponds to a read-only address (or has no parameters) then the data is ignored

**Figure 5-17: Dialog SPI Read Command with parameters**

The 6-bit ID code (see Table 5-9 below) is stored in the SERID register 0xC2, and is shared with the I<sup>2</sup>C interface.

**Table 5-9: SERID register details**

Address	OTP	Name	Type	Bit Values								Initial Value
				b7	b6	b5	b4	b3	b2	b1	b0	
0xC2	Yes	SERID (Serial Interface ID)	W	0	0							0x00

**Figure 5-18: Dialog SPI Paused Read Command**

## 5.9 2-wire Serial ( $I^2C$ )

The DA8620 2-wire SPI ( $I^2C$ ) mode is a 400 kbit/s slave. Although it operates at a fraction of the SPI speed, it has the same feature set as any of the other 8-bit serial interfaces, as all functions are accessed through the same standard command set.

The **SDA\_SDO** pin is placed in open drain configuration by making SPB and MPU[1:0] externally tied high and RWB\_WRB\_SPI externally tied low.

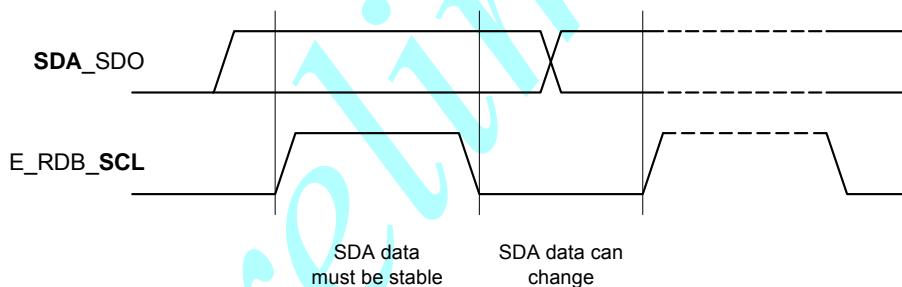
**Table 5-10:  $I^2C$  Mode Signals**

Pad Name	Type	Description
RSTB	I	Asynchronous Reset
CSB	I	Chip Select is not used and can be left unconnected
DCB	I	Data / Command Select is not used and can be left unconnected
RWB_WRB_SPI	I	Must be set to 0 to select $I^2C$ mode
E_RDB_SCL	I	Serial Clock
SDI	I	Serial Data In is not used
<b>SDA_SDO</b>	I/O	Serial Data In/Out (open drain)
SPB	I	Must be set to 1 to select serial interface mode
MPU[1:0]	I	Must be set to 0x3 (binary 11) to select $I^2C$

Notes (see also Figure 5-19):

1. The **SDA\_SDO** data must be stable during the high period of the **E\_RDB\_SCL** clock.
2. **SDA\_SDO** data can only be changed when the **E\_RDB\_SCL** clock is low.

**Figure 5-19:  $I^2C$  Data States**



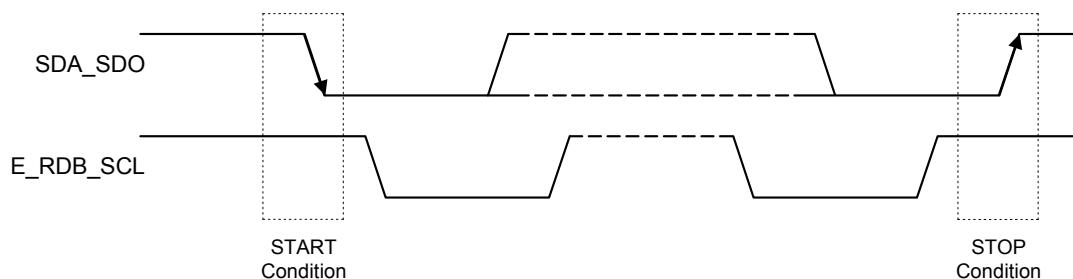
The START and STOP detections are determined by the Master setting the **SDA\_SDO** and **E\_RDB\_SCL** signals to unique conditions:

START:A negative edge on **SDA\_SDO** when **E\_RDB\_SCL** is HIGH

STOP:A positive edge on **SDA\_SDO** when **E\_RDB\_SCL** is HIGH.

These conditions are shown below in Figure 5-20.

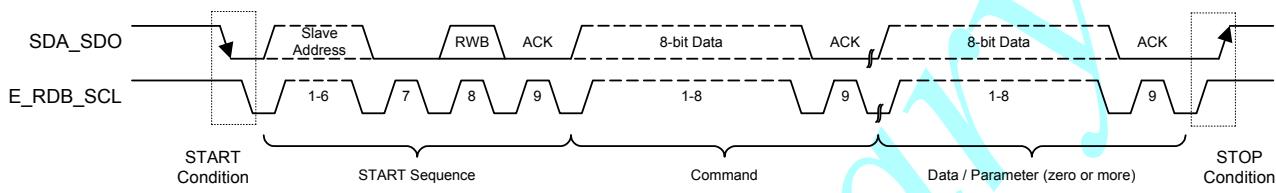
**Figure 5-20:  $I^2C$  Start Stop conditions**



The 8-bit start byte consists of a 7-bit slave device address and a read/write selection bit, RWB. Since the DA8620 only performs as a slave in the I<sup>2</sup>C mode, the LSB of the slave device address is fixed to 0, and only the upper 6 bits are configurable. The I<sup>2</sup>C mode takes its address from the same SERID register (see Table 5-9) as the Dialog SPI mode described above.

If the Slave Device address matches the transmitted 6-bit address, the DA8620 will send an acknowledgement (ACK) to the host, by pulling SDA\_SDO low during the 9<sup>th</sup> E\_RDB\_SCL clock pulse. All subsequent transfers will also be acknowledged.

**Figure 5-21: I<sup>2</sup>C Data Transfer sequence**

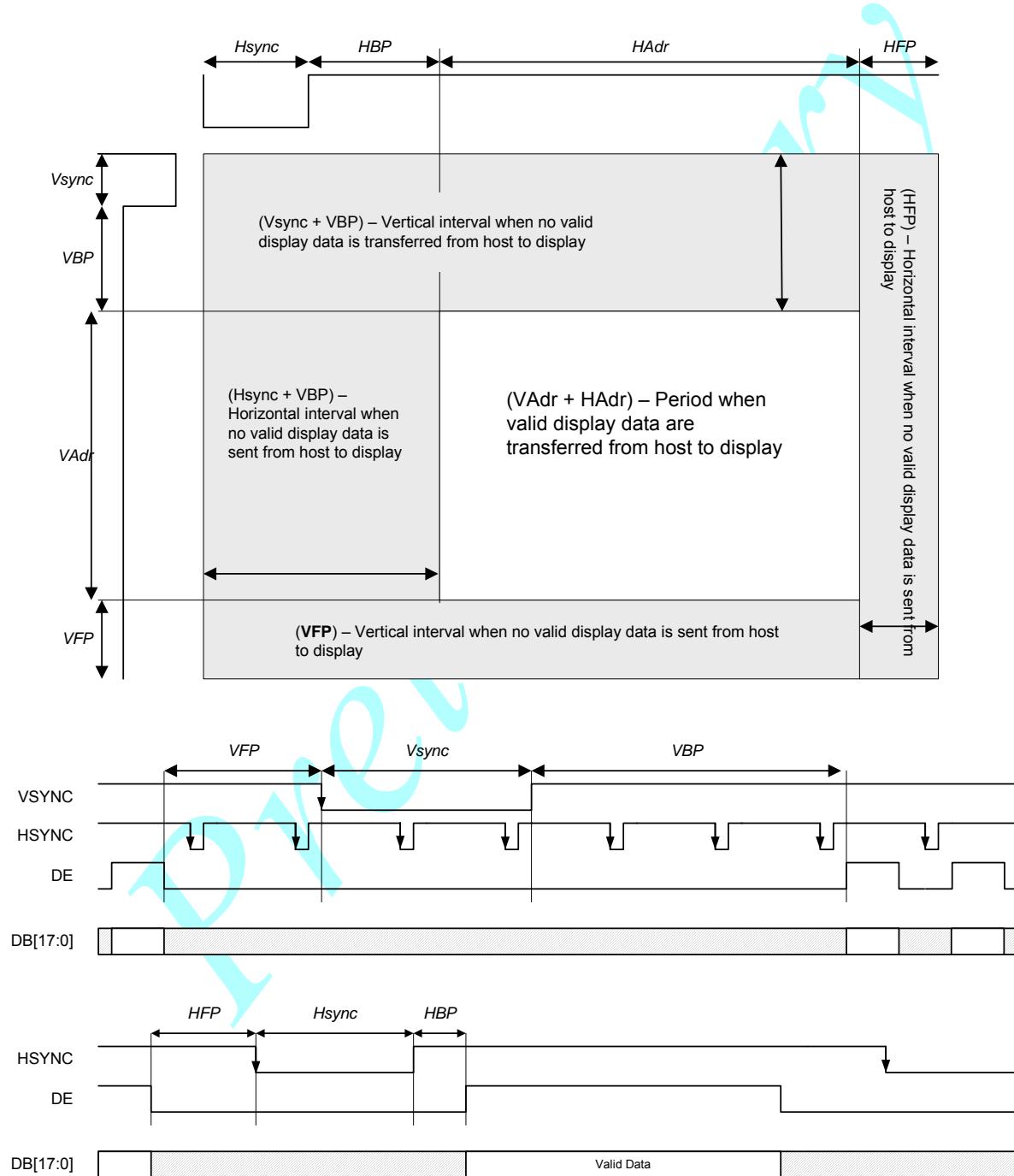


## 6: RGB Interface

### 6.1 Introduction

The RGB interface is selected when the SPB pad is high. The framing of data in the RGB mode is shown below:

**Figure 6-1: RGB Framing**



Notes:

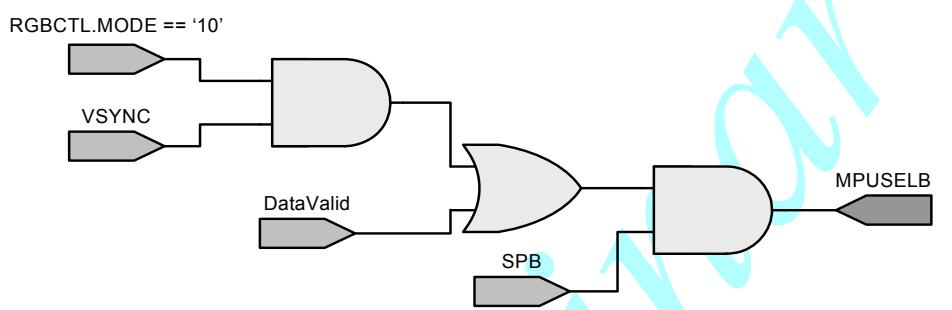
- (1) There is no hard requirement for VSYNC to be coincident with HSYNC (above taken from Nokia DMIF-S50AP-T22 spec).
- (2) If VSYNC and HSYNC are not coincident then we will need to align internally for RSYNC generation.

There are two schemes for defining the active region of the display:

1. Use the DE pin to identify valid data and the edge of the HSYNC and VSYNC signals to synchronize frames and identify new lines.
2. Define the region of interest using CASET (Register 0x2A) and PASET (Register 0x2B).

It is not possible to write to the display RAM through the RGB interface and MPU interface at the same time. A mechanism is therefore needed to guarantee that only one interface has exclusive access at a time. Accordingly, priority is assigned to the RGB interface, such that it has exclusive access when its data is valid. Any data transferred through the MPU interface at such times will be ignored.

**Figure 6-2: MPU Select Signal (active low)**



The default active levels of the VSYNC, HSYNC, and DE signals are shown in Figure 6-1. These can be inverted using RGBCTL[4:2] (Register 0xC1). All RGB interface signals should be retimed using the rising edge of PCLK before being used. The register bits RGBCTL[7:5] can be used to retime these signals to the falling edge of PCLK to accommodate any delays in transmission (sometimes the data is multiplexed with GPIO pins and is thus delayed relative to the clock).

**Table 6-1: RGBCTL (0xC1) Register Details**

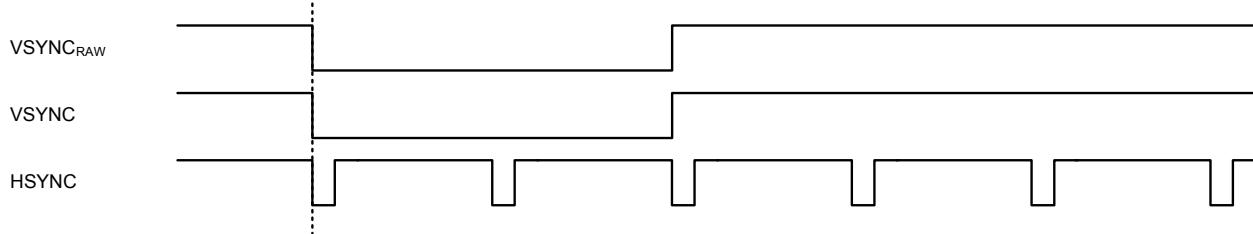
Address	OTP	Name	Type	Bit Values								Initial Value			
				b7	b6	b5	b4	b3	b2	b1	b0				
0xC1	Y	RGBCTL (RGB Control)	W	D7	D6	D5	D4	D3	D2	MODE		0x01			
				where:											
				D7	Syncs latched on falling edge of PCLK										
				D6	DE latched on falling edge of PCLK										
				D5	Data latched on falling edge of PCLK										
				D4	VSYNC active high										
				D3	HSYNC active high										
				D2	DE active low										
				MODE:											
				00	Ignore DE pin										
				01	DE defines Valid Data										
				10	DE defines Active Area										
				11	Reserved										

**Data Valid**

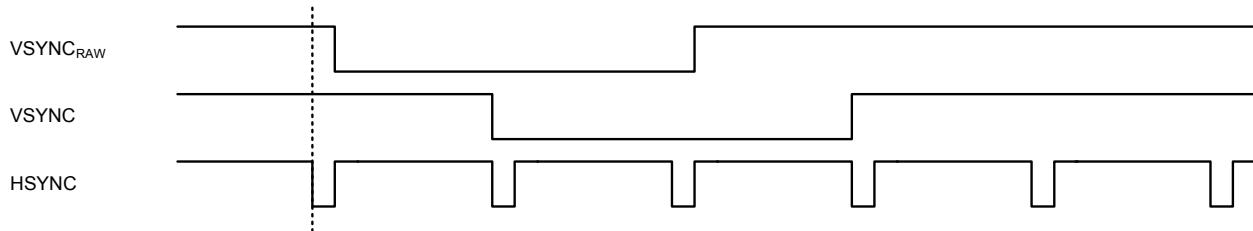
Data is defined as being valid when all three control signals are active - that is DE, HSYNC, and VSYNC. The active polarity of the control signals can be inverted through the RGBCTL (0xC1) register. VSYNC is internally resynchronized to HSYNC as shown below.

**Figure 6-3: VSYNC re-sampling**

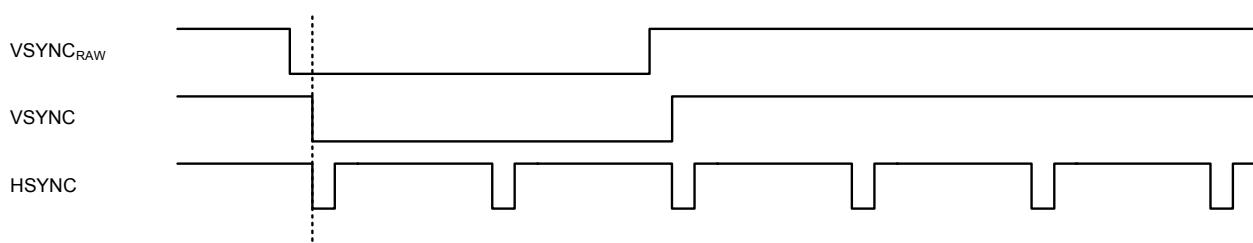
(i)  $\text{VSYNC}_{\text{RAW}}$  Coincident with neg edge of HSYNC



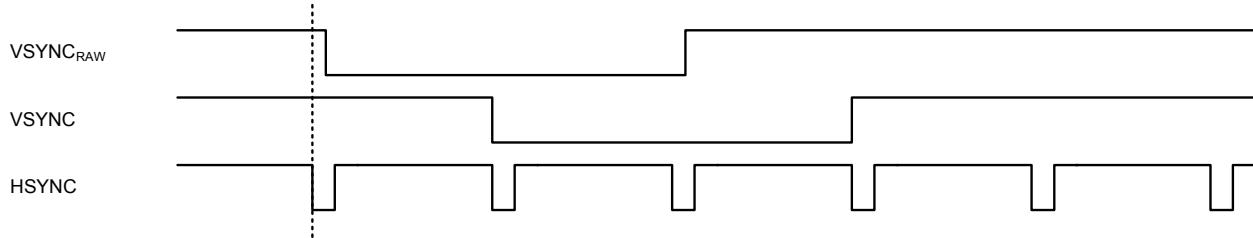
(ii)  $\text{VSYNC}_{\text{RAW}}$  Coincident with pos edge of HSYNC

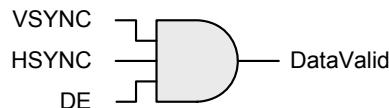


(iii)  $\text{VSYNC}_{\text{RAW}}$  during HSYNC active period

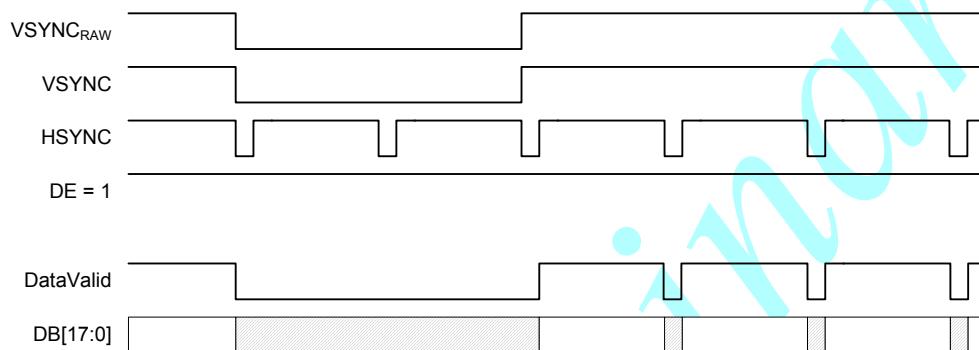
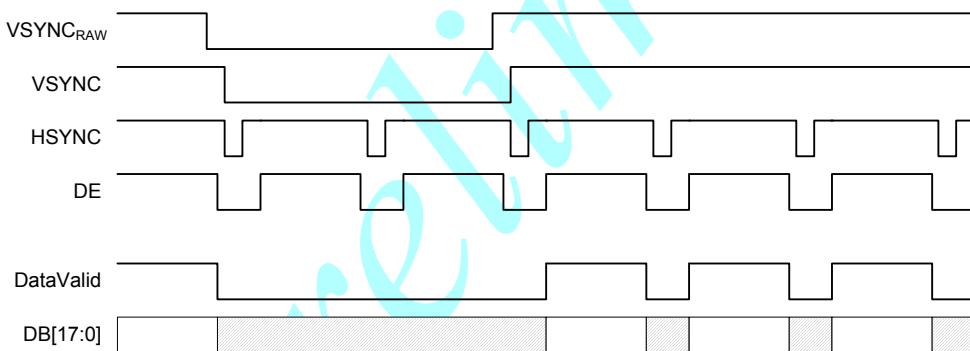
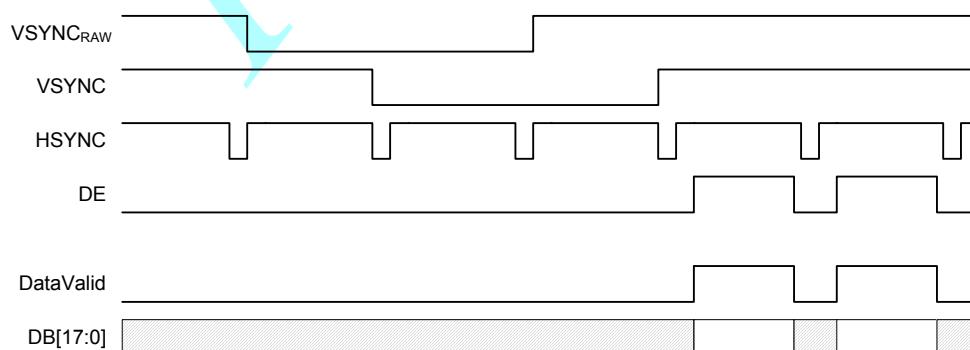


(iv)  $\text{VSYNC}_{\text{RAW}}$  during HSYNC blanking period



**Figure 6-4: Data valid generation**

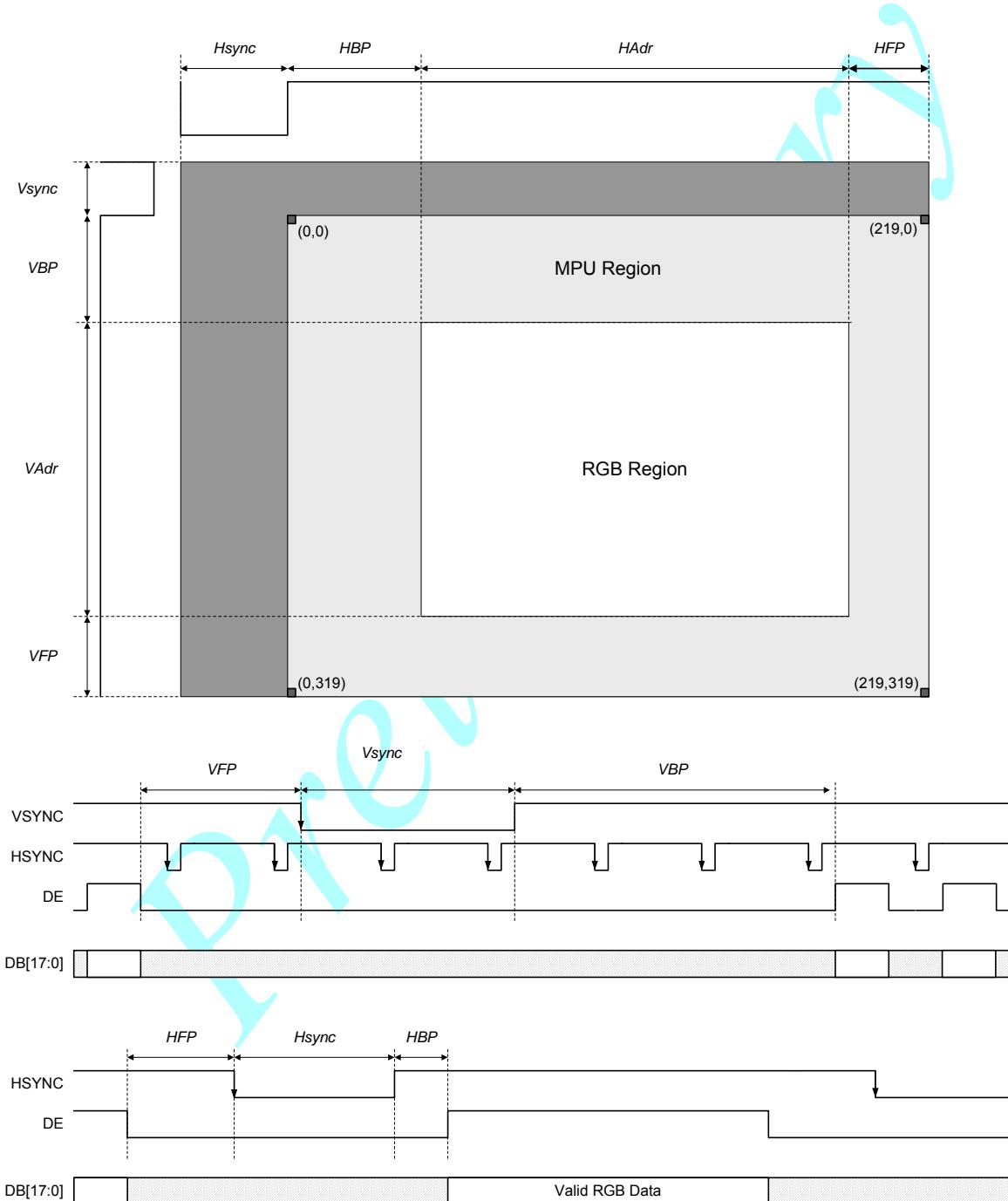
The action of the DE pin is defined by the MODE field of the RGBCTL (0xC1) register. If the mode is defined to ignore the DE pin then valid data is determined by the HSYNC and VSYNC signals alone. If the MODE field of the RGBCTL (0xC1) register is defined such that the DE pin defines either "valid data" or "active area" then the DE pin determines the validity of the data.

**Figure 6-5: RGB Mode - Ignore DE Pin****Figure 6-6: RGB Mode - DE Pin Defines Valid Data****Figure 6-7: RGB Mode - DE Pin Defines Active Area**

## 6.2 Windowing

As per the MPU mode, the RGB mode recognizes the window as defined by the CASET (0x2A) and PASET (0x2B) registers. The contents of these registers are sent to the anodes at the start of every new frame. The "DE pin defines Active Area" mode RGBCTL[1:0] = 10 defines a sub-window within this window as shown in Figure 6-8. The "DE pin defines Valid Data" mode RGBCTL[1:0] = 01 simply uses the MPU region.

**Figure 6-8: Combined Video and Still Windowing**



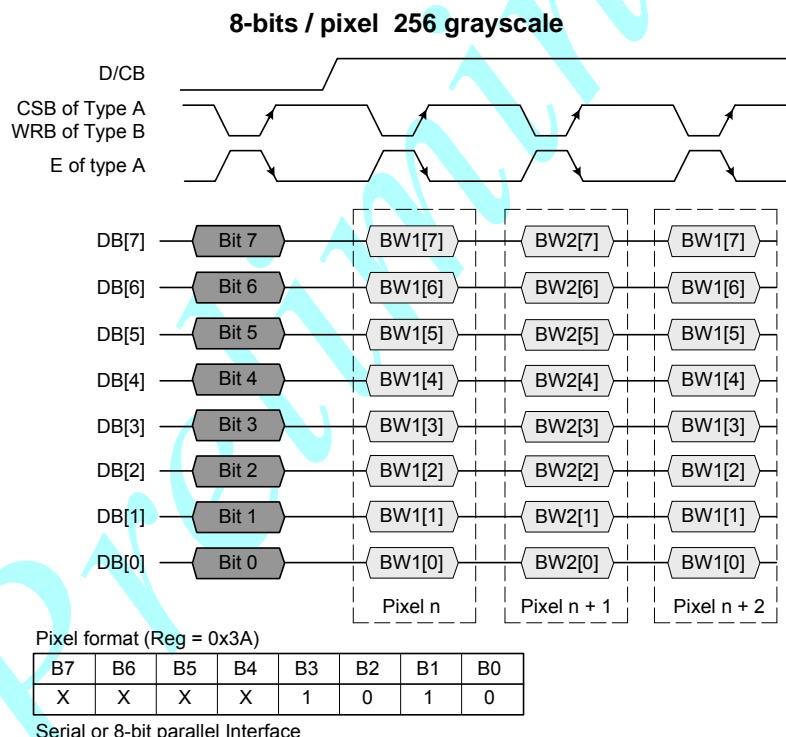
**Table 6-2: RGB Update Rules (NDMIF)**

Condition	Horizontal Counter	Vertical Counter
An active VSYNC is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HSYNC signal between two active area lines	Return to 0	Increment by 1
The horizontal counter value is greater than 239 and the vertical counter value larger than 319	Return to 0	Return to 0

When operating within a window, as defined by CASET and PASET, the numbers in the above table should be considered to be the limits defined by the registers. The decision to increment or decrement will be determined by the MADCTL (0x36) register.

### 6.2.1 RGB to Grayscale Conversion

The DA8620 provides an 8-bit data / 8-bit interface mode for monochrome displays through the normal MIPI pixel encodings. This mode assumes that the source material has already been converted into 8-bit gray scales

**Figure 6-9: Grayscale mode**

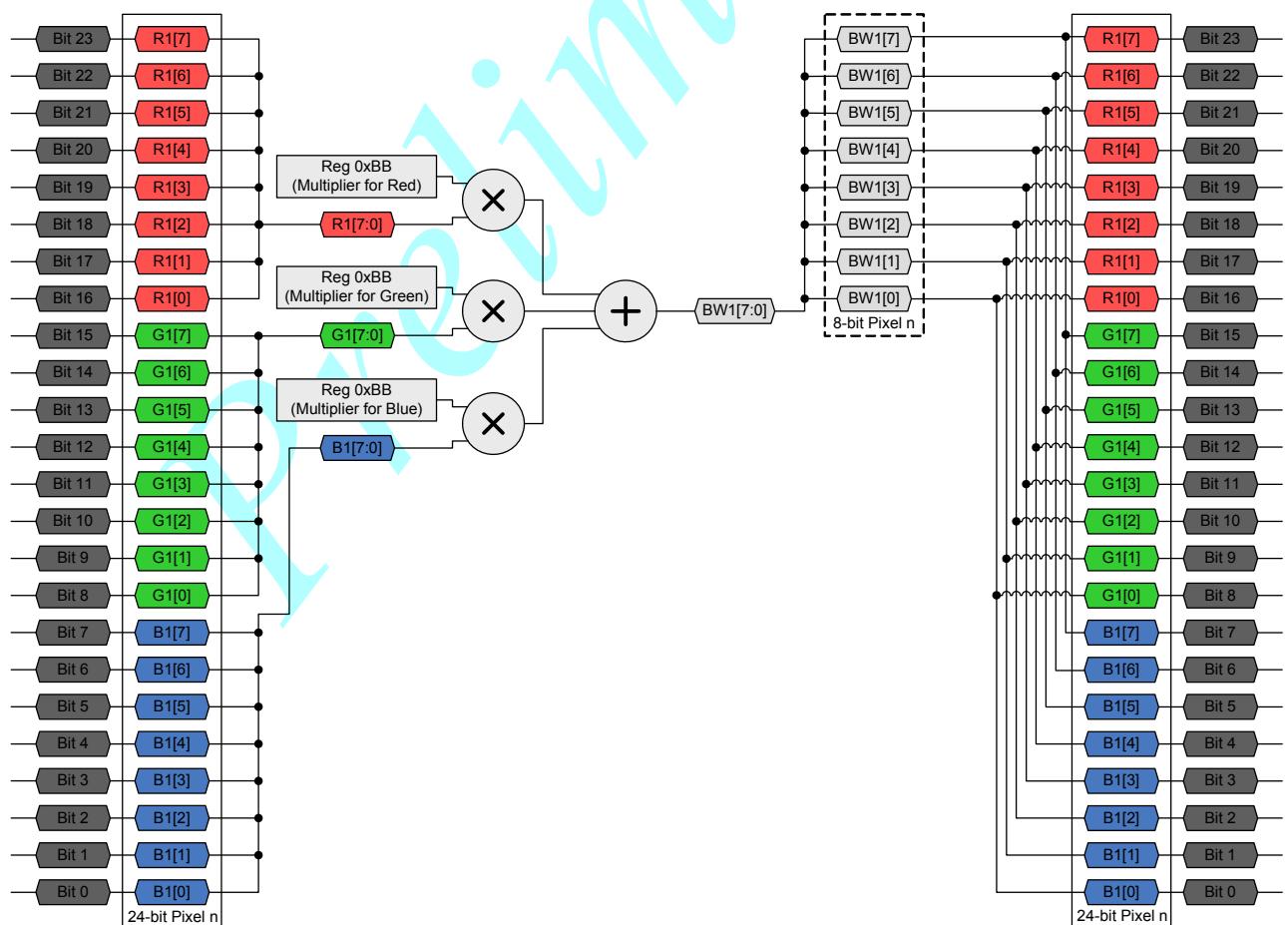
The DA8620 also has the ability to convert automatically any RGB data into monochrome data.

The BW bit in the DCSCTL (0xC0) register will automatically convert an RGB image into a grayscale image using the multipliers stored in the BWCONV (0xBB) register. It is important that the sum of these three multipliers equals 0x100. The default multipliers are Red = 30% (0x4D / 0x100), Green = 59% (0x77 / 0x100), and Blue = 11% (0x1C / 0x100). The conversion happens just before the Gamma correction is applied.

Table 6-3: Grayscale Control Registers

Address	OTP?	Name	Type	Bit values								Initial value			
				B7	B6	B5	B4	B3	B2	B1	B0				
0xBB	Yes	BWCONV (Black/white convert)	W	Multiplier for Red								0x4D			
				Multiplier for Green								0x97			
				Multiplier for Blue								0x1C			
0xC0	Yes	DCSCTL (DCS Control)	W	BW	BM	CS	CH	TE	SG	RGB OPT	MPU OPT	0x10			
				0	0	0	0	0	0	0	0	0x00			
where:															
BW    Black and White convert															
BM    Bottom Mount device															
CS    Clear Memory on SW Reset															
CH    Clear Memory on HW Reset															
TE    Output RSYNC on the TE pin															
SG    A single Gamma Table															
D1    RGBOPT for Pixel Format															
D0    MPUOPT for Pixel Format															

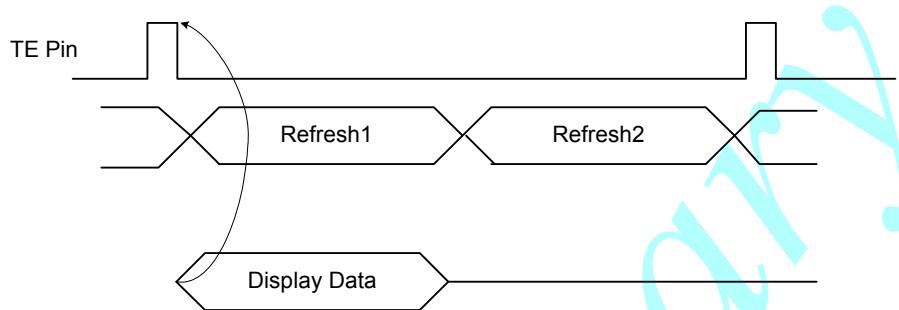
Figure 6-10: 24-bits/pixel, RGB to Grayscale Convert



### 6.2.2 Tearing Effect

The DA8620 has a double-buffered architecture that allows the handling of high speed video streaming data without a tearing effect. The traditional synchronous method of sending the Display RAM data by scanning the TE (tearing effect) pin is one of the various methods available. The examples below use 2 refresh rates per image displayed

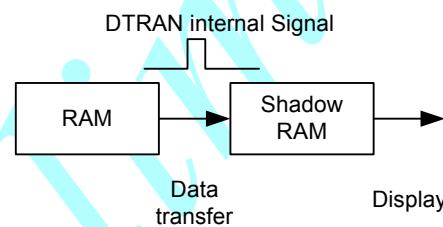
**Figure 6-11: TE Pin Synchronizing**



The TE pin is accessible, can be scanned, and the Display Data should always be written after each falling edge of TE pin. This is a classical method to make sure tearing is avoided.

The DA8620 incorporates special modes that allow the sending of display data without synchronizing to the TE pin (which is a real burden for the application processor). This method is made possible by the double-buffered architecture.

**Figure 6-12: Double-buffered Architecture**



The display data can be written to the RAM at any time. After sending the display data, the processor can send a DTRAN command that will start the data transfer from the RAM to the shadow RAM at a multiple of the refresh rate (for further information, please refer to the Application Note).

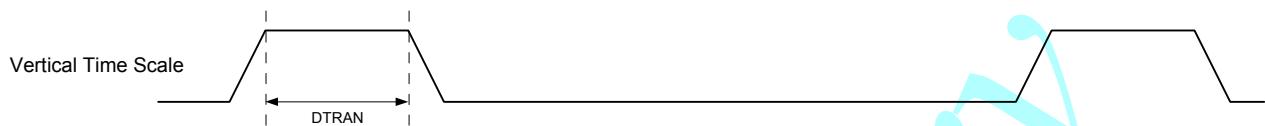
#### 6.2.2.1 Tearing Effect Signals

The tearing effect operation is defined by the TEON (0x35), TEOFF (0x34) and TESLSET (0x44) commands. The DA8620 must support both V-Blanking only mode and the combined V- and H-Blanking modes. In this mode the width of the V-Blanking pulse is defined by the DTRAN time (which should also be identical to the RSYNC pulse). The H-Blanking pulse is fixed at 4 system clocks.

**Figure 6-13: Different Tearing Effect Modes**

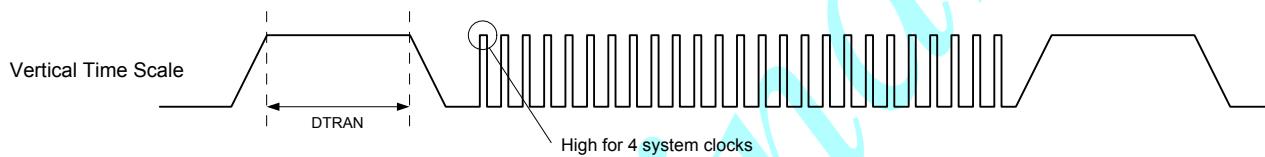
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:



The TESLSET (0x44) command defines the Tearing Effect signal as a horizontal line count offset from the start of the frame. This overrides the TEON mode to force the signal to be V-Blanking only. When the scan line is non-zero the width of the V-Blanking pulse remains DTRAN but is offset by the specified number of HSYNC lines.

**Figure 6-14: Tearing Effect Scan Line Set**

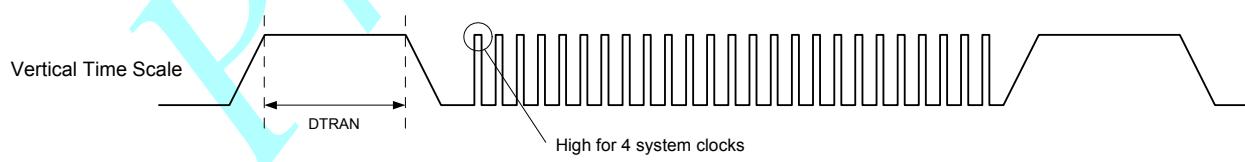
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:



### 6.2.3 Data Mapping

The COLMOD (0x3A) command defines the pixel format. The register encoding is compatible with the MIPI-DCS spec. The MPUOPT and RGBOPT bits are set through the DCSCTL (0xC0) register.

**Table 6-4: Data Mapping Control Registers**

Address	OTP	Name	Type	Bit Values								Initial Value				
				b7	b6	b5	b4	b3	b2	b1	b0					
0x3A	Yes	COLMOD (Set Display Pixel Format)	W	0	RGBPF[2:0]			0	MPUPF[2:0]			0x67				
				where: xxxPF is given by the following table:												
				000	Reserved											
				001	Reserved											
				010	8 bits/pixel											
				011	12 bits/pixel											
				100	Reserved											
				101	16 bits/pixel											
				110	18 bits/pixel											
				111	24 bits/pixel											
0xC0	Yes	DCSCTL (DCS Control)	W	0	0	CS	CH	TE	SG	RGB OPT	MPU OPT	0x00				
				where:												
				CS	Clear Memory on SW Reset											
				CH	Clear Memory on HW Reset											
				TE	Output RSYNC on the TE pin											
				SG	A single Gamma Table											
				D1	RGBOPT for Pixel Format											
				D0	MPUOPT for Pixel Format											

The mapping of pixel format to DA8620 interface (and the number of transfers required per pixel) is given by the following table.

**Table 6-5: Pixel Formats**

Pixel Format	Description	8-bit 8068-mode SPI & I <sup>2</sup> C		16-bit 80-mode 16-bit 68-mode		18-bit RGB	
		Option 1	Option 2	Option 1	Option 2	Option 1	Option 2
000	reserved	---	---	---	---	---	---
001	reserved	---	---	---	---	---	---
010	8 bits/pixel	8 bits	8 bits	16 bits (1/2 txf)	---	16 bits (2 txf)	8 bits
011	12 bits/pixel	8 bits (3/2 txf)	---	12 bits	---	12 bits	8 bits (3/2 txf)
100	reserved	---	---	---	---	---	---
101	16 bits/pixel	8 bits (2 txf)	8 bits (2 txf)	16 bits	---	16 bits	8 bits (2 txf)
110	18 bits/pixel	9 bits (2 txf)	9 bits (2 txf)	16 bits (3/2 txf)	16 bits (2 txf)	18 bits (1 txf)	6 bits (3 txf)
111	24 bits/pixel	8 bits (3 txf)	---	16 bits (3/2 txf)	16 bits (2 txf)	16 bits (3/2 txf)	8 bits (3 txf)

Notes:

- (a) The reserved mappings are treated as 8 bits/pixel
- (b) If option 2 is not defined then the encoding defaults to option 1
- (c) Option 1 is encoded as "0" in the RGB\_OPT and/or MPU\_OPT bits
- (d) The 18 bits/pixel encoding of 8-bit bus in parallel mode is 9-bits
- (e) The 18 bits/pixel encoding of 8-bit bus is not valid in the SPI and I<sup>2</sup>C modes
- (f) txf refers to interface transmit frames.

### 6.2.3.1 8-bit Bus Interface

There are five possible combinations of data formats that are valid for the 8-bit interface. If no explicit option number is given then the option 1 encoding is assumed.

**Figure 6-15: 8-bit bus data formats**

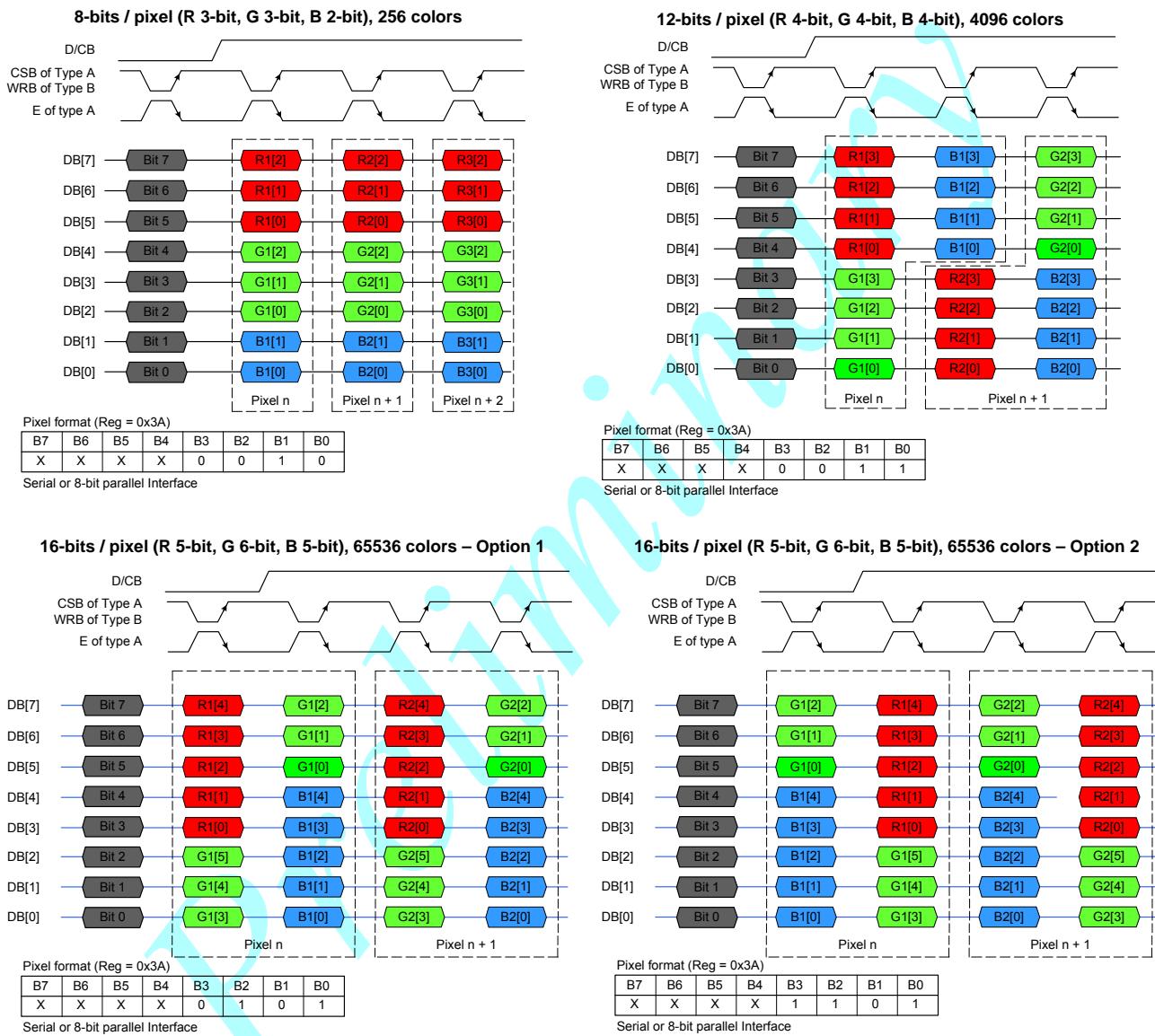
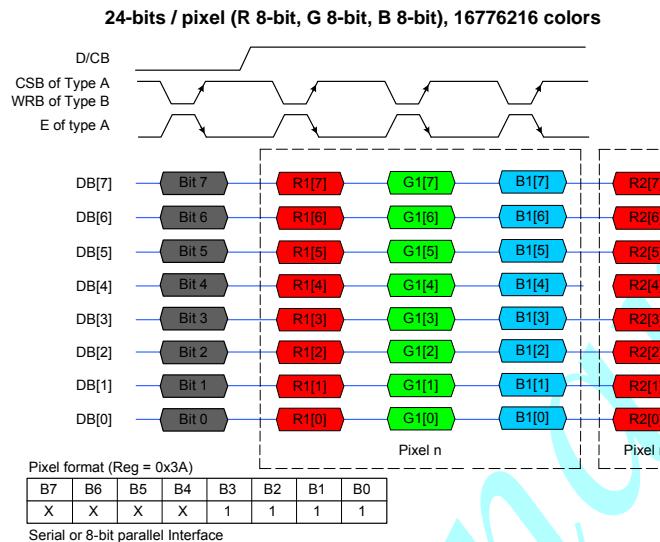


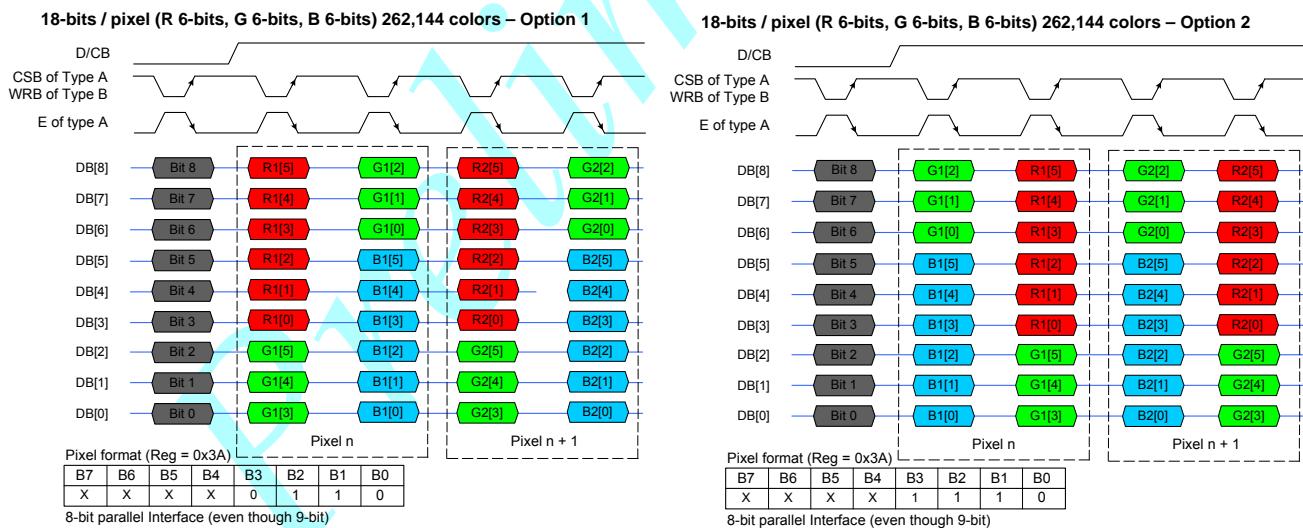
Figure 6-15: 8-bit bus data formats (continued)



### 6.2.3.2 9-bit Bus Interface

There are two valid data formats in this mode. As the MPU encoding bits only allow for 8-bit and 16-bit encoding, the 9-bit bus is activated by selecting the 18-bits/pixel format in the 8-bit MPU mode.

Figure 6-16: 9-bit bus data formats

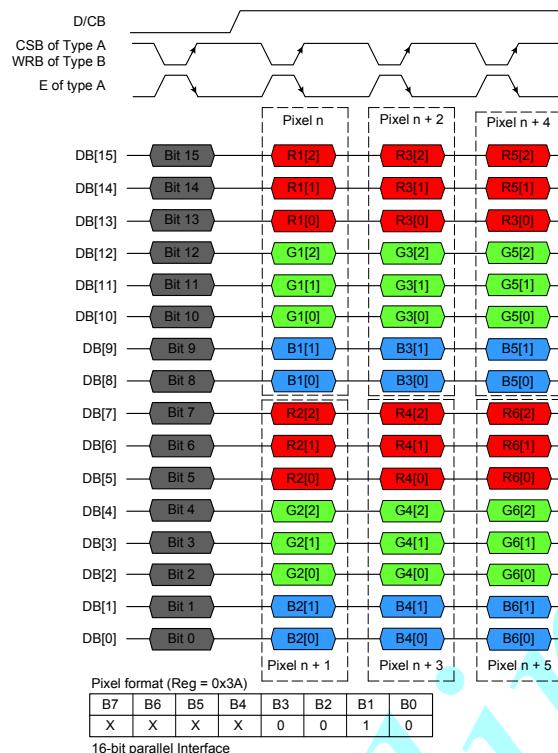


### 6.2.3.3 16-bit Interface

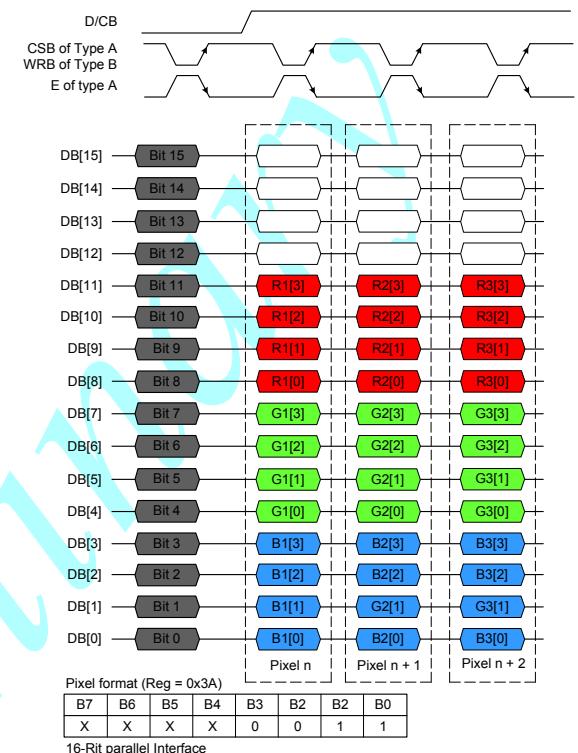
The 16-bit interface can support all pixel formats, as shown below in Table 6-6.

**Table 6-6: 16-bit bus data formats**

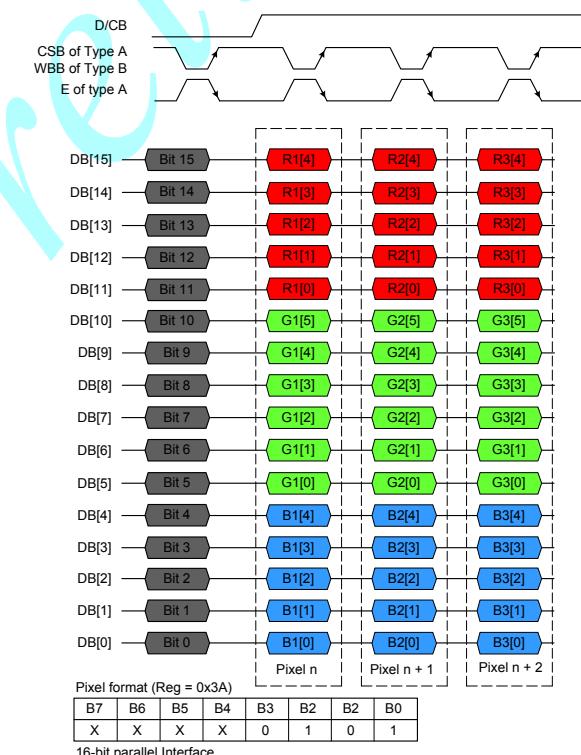
#### 16-bit Interface: 8-bits / pixel (R 3-bit, G 3-bit, B 2-bit), 256 colors



#### 16-bit Interface: 12-bits / pixel (R 4-bit, G 4-bit, B 4-bit), 4096 colors

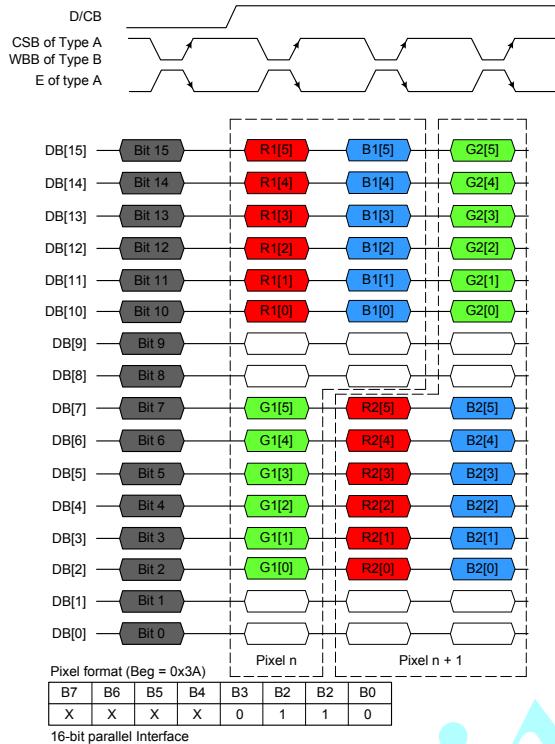


#### 16-bit Interface: 16-bits / pixel (B 4-bit, G 5-bit, b 4-bit), 65536 colors

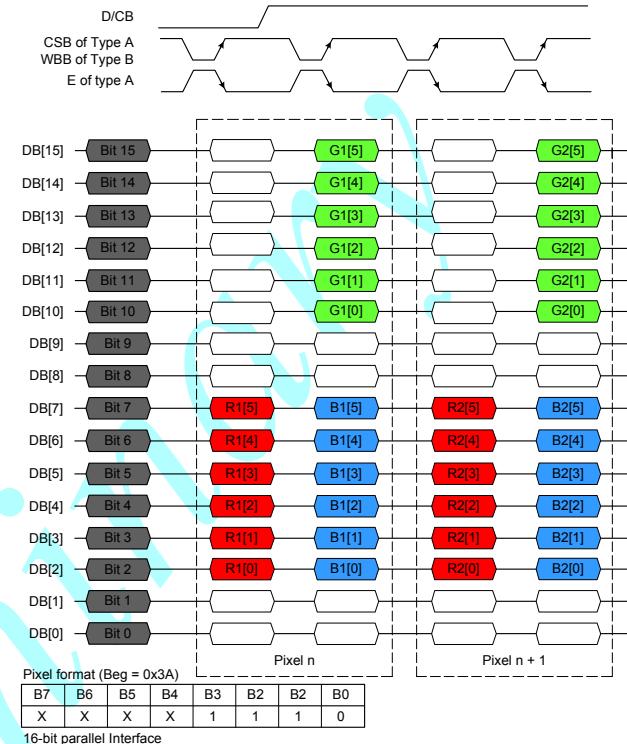


**Table 6-6: 16-bit bus data formats (continued)**

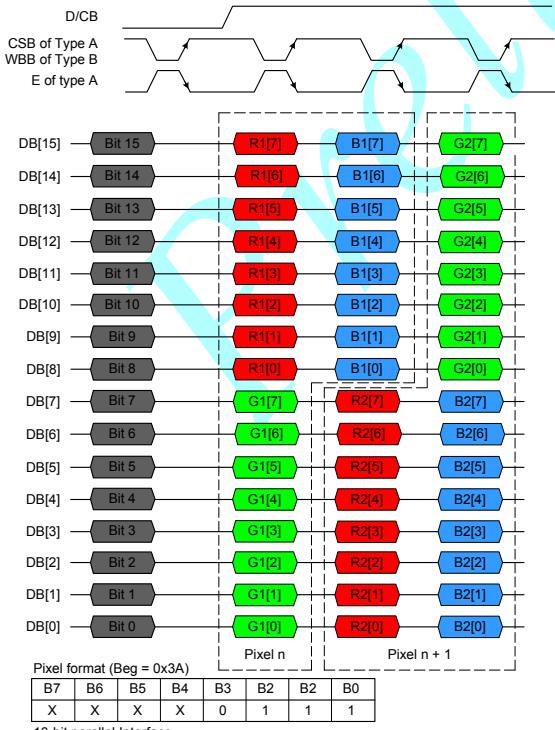
**16-bit Interface: 18-bits / pixel (B 6-bit, G 6-bit, b 6-bit), 262,144 colors**  
Option 1



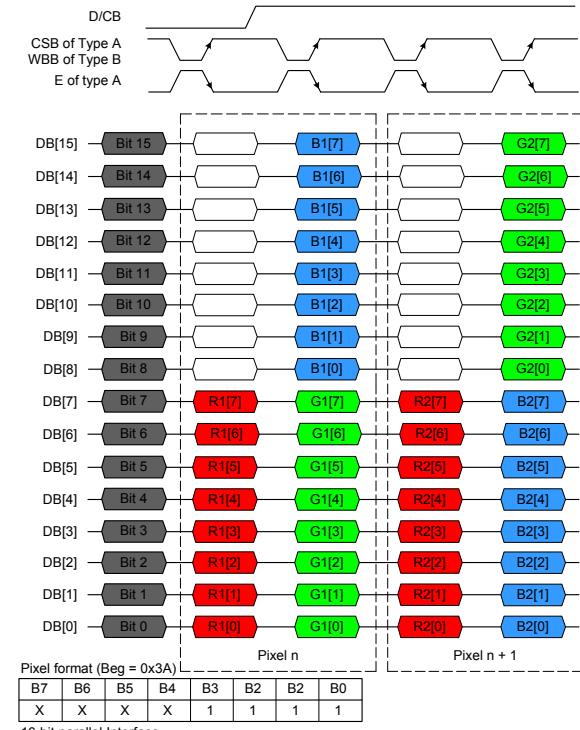
**16-bit Interface: 18-bits / pixel (B 6-bit, G 6-bit, b 6-bit), 262,144 colors**  
Option 2



**16-bit Interface: 24-bits / pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors** Option 1



**16-bit Interface: 24-bits / pixel (R 8-bit, G 8-bit, B 8-bit), 16,777,216 colors** Option 1

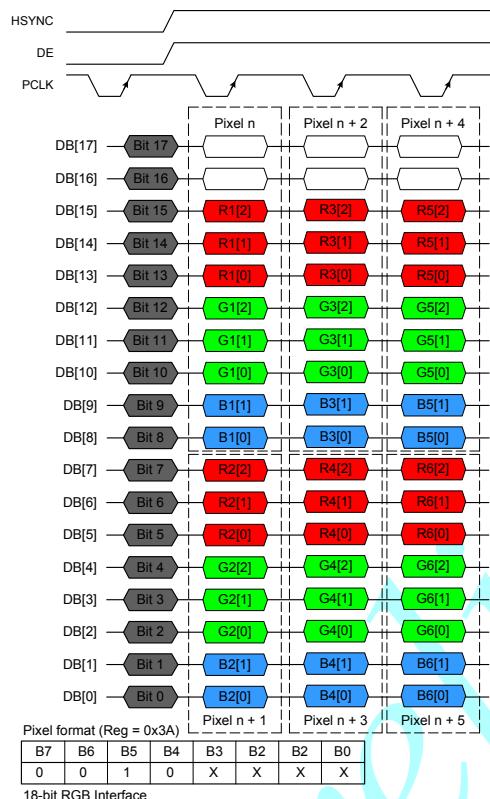


### 6.2.3.4 18-bit Interface

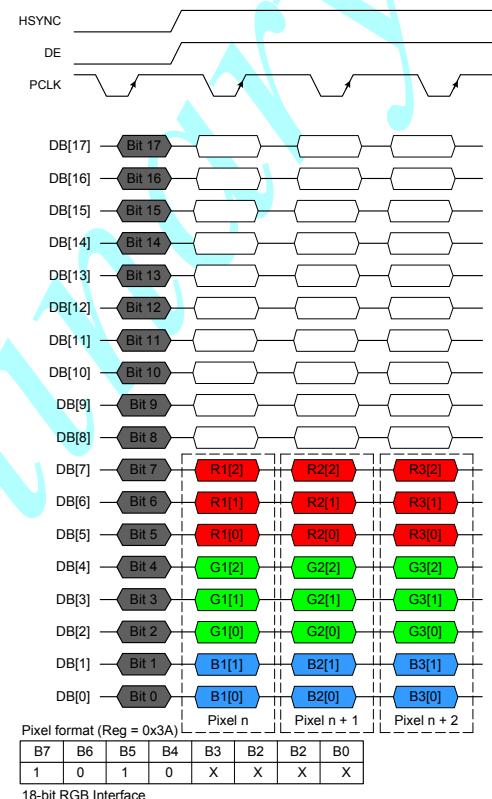
The 18-bit interface is only valid for the RGB (DPI) port, the majority of the pixel formats are identical to those used with the 8- and 16-bit interface, with the top two bits ignored. When packed pixels are sent (i.e. the 24-bit Option 2) the transfer is re-synchronised at the start of a frame.

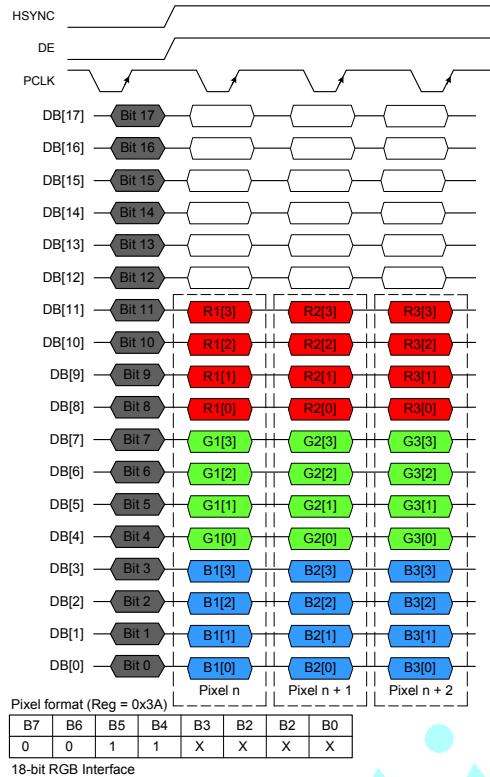
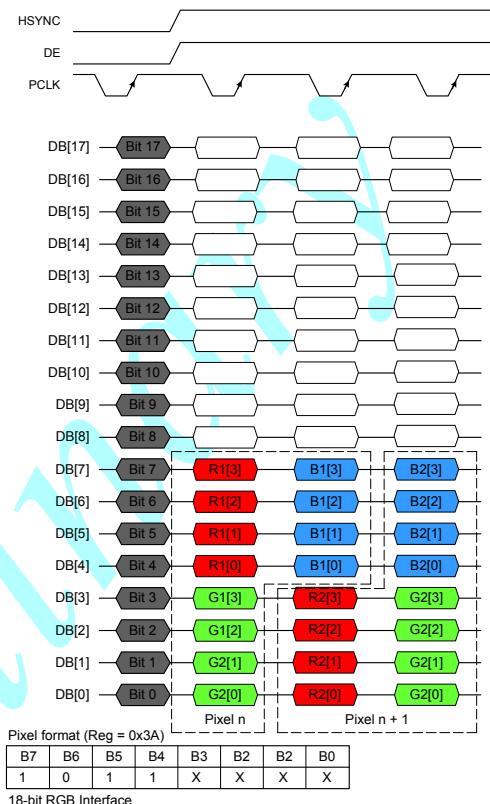
**Table 6-7: 18-bit bus data formats**

**18-bit Interface: 8-bits / pixel (R 3-bit, G 3-bit, B 2-bit), 256 colors**  
Option 1



**18-bit Interface: 8-bits / pixel (R 3-bit, G 3-bit, B 2-bit), 256 colors**  
Option 2



**Table 6-7: 18-bit bus data formats (continued)****18-bit Interface: 12-bits / pixel (R 4-bit, G 4-bit, B 4-bit), 4096 colors  
Option 1****18-bit Interface: 12-bits / pixel (R 4-bit, G 4-bit, B 4-bit), 4096 colors  
Option 2**

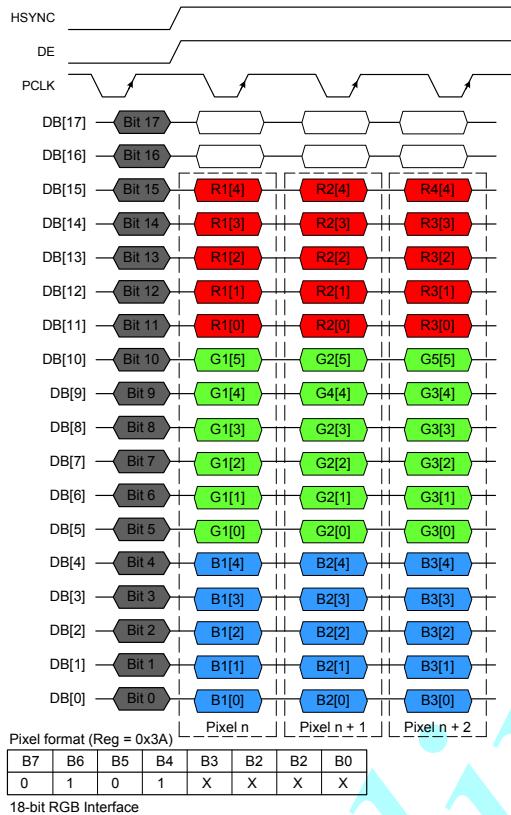
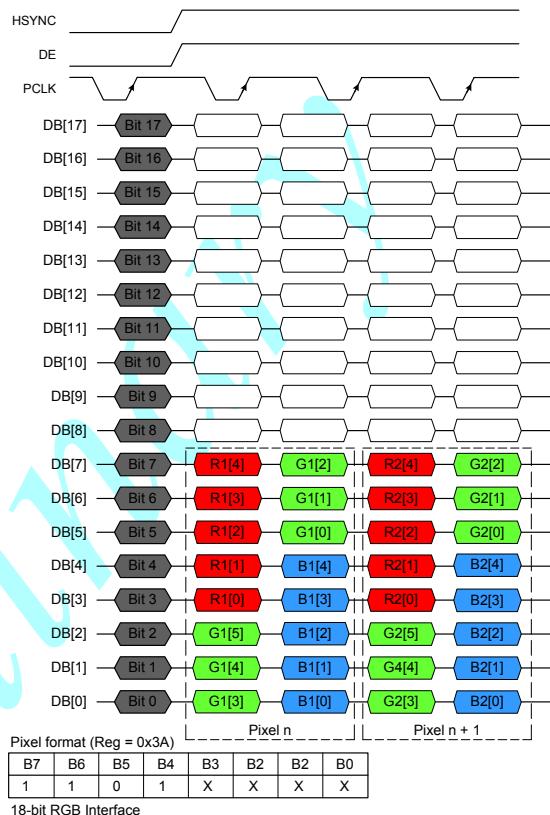
**Table 6-7: 18-bit bus data formats (continued)****18-bit Interface: 16-bits / pixel (R 5-bit, G 6-bit, B 5-bit), 65536 colors  
Option 1****18-bit Interface: 16-bits / pixel (R 5-bit, G 6-bit, B 5-bit), 65536 colors  
Option 2**

Table 6-7: 18-bit bus data formats (continued)

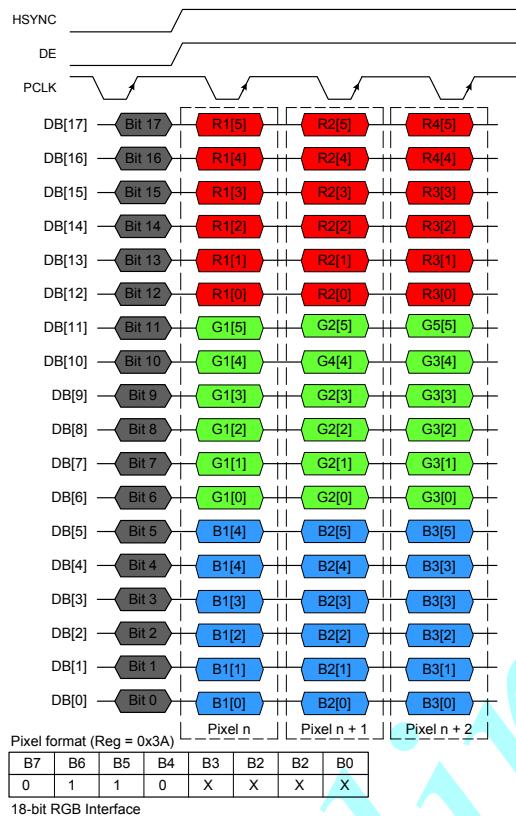
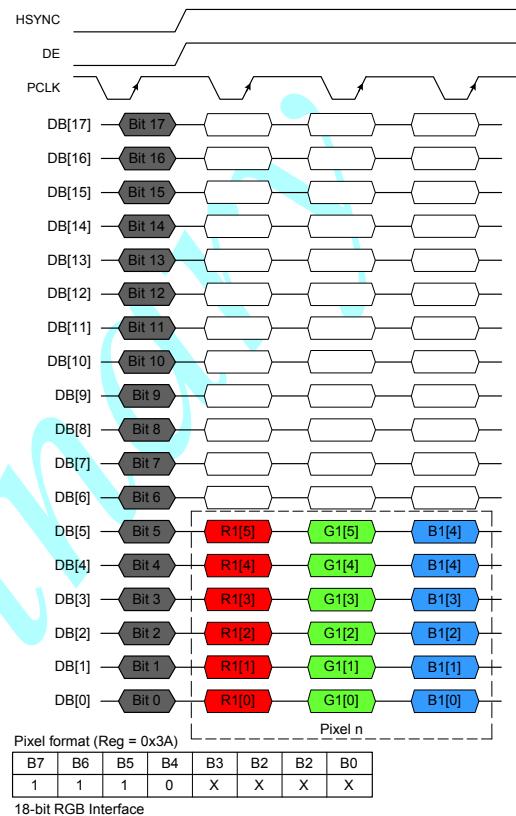
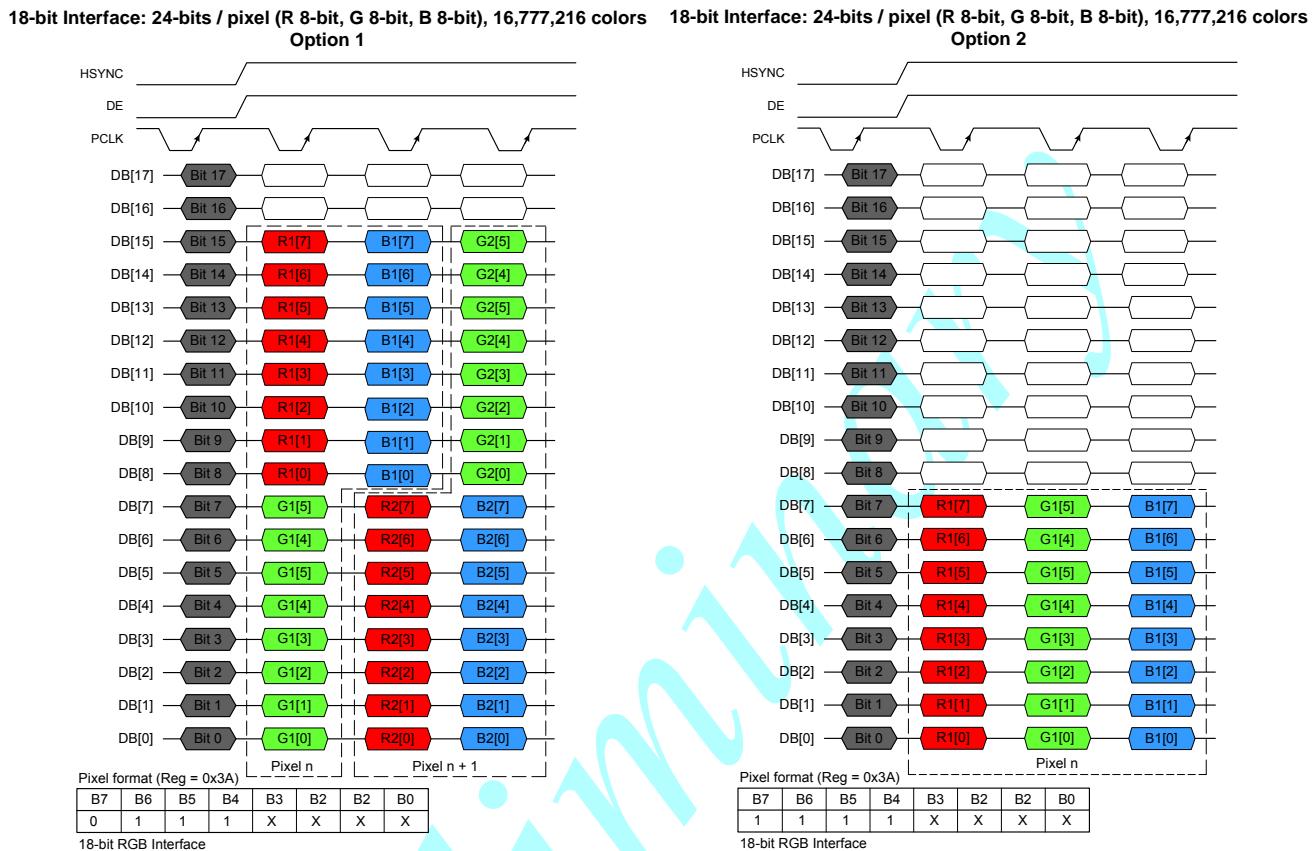
18-bit Interface: 16-bits / pixel (R 5-bit, G 6-bit, B 5-bit), 65536 colors  
Option 118-bit Interface: 16-bits / pixel (R 6-bit, G 6-bit, B 6-bit), 262,144 color  
Option 2

Table 6-7: 18-bit bus data formats (continued)



### 6.2.4 Pixel Mapping to 24-bits

The mapping to 24-bits is achieved by replicating the most-significant bits of the original data, thus providing a smoother transition from 0 to 255.

**Table 6-8: 24-bit bus data formats**

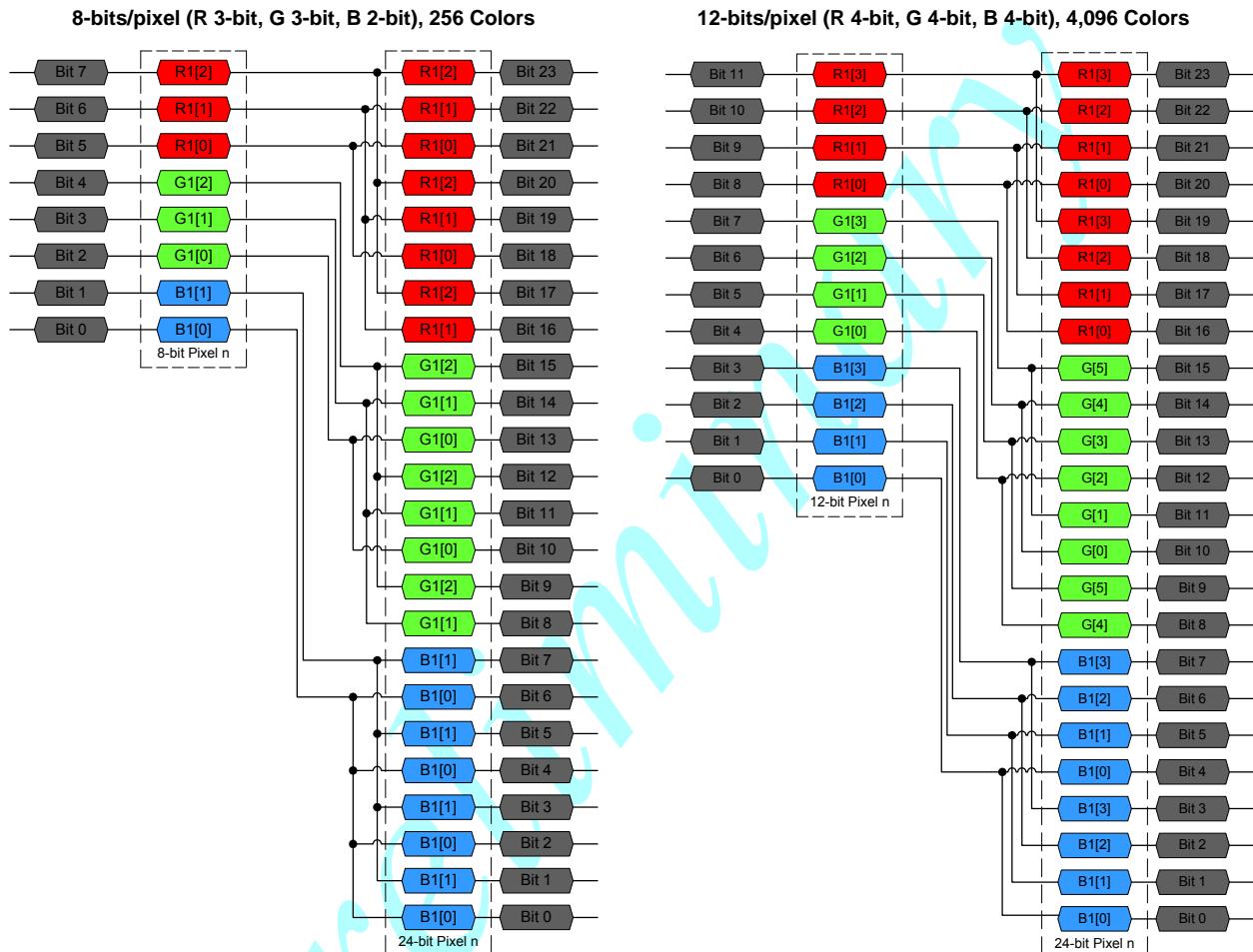
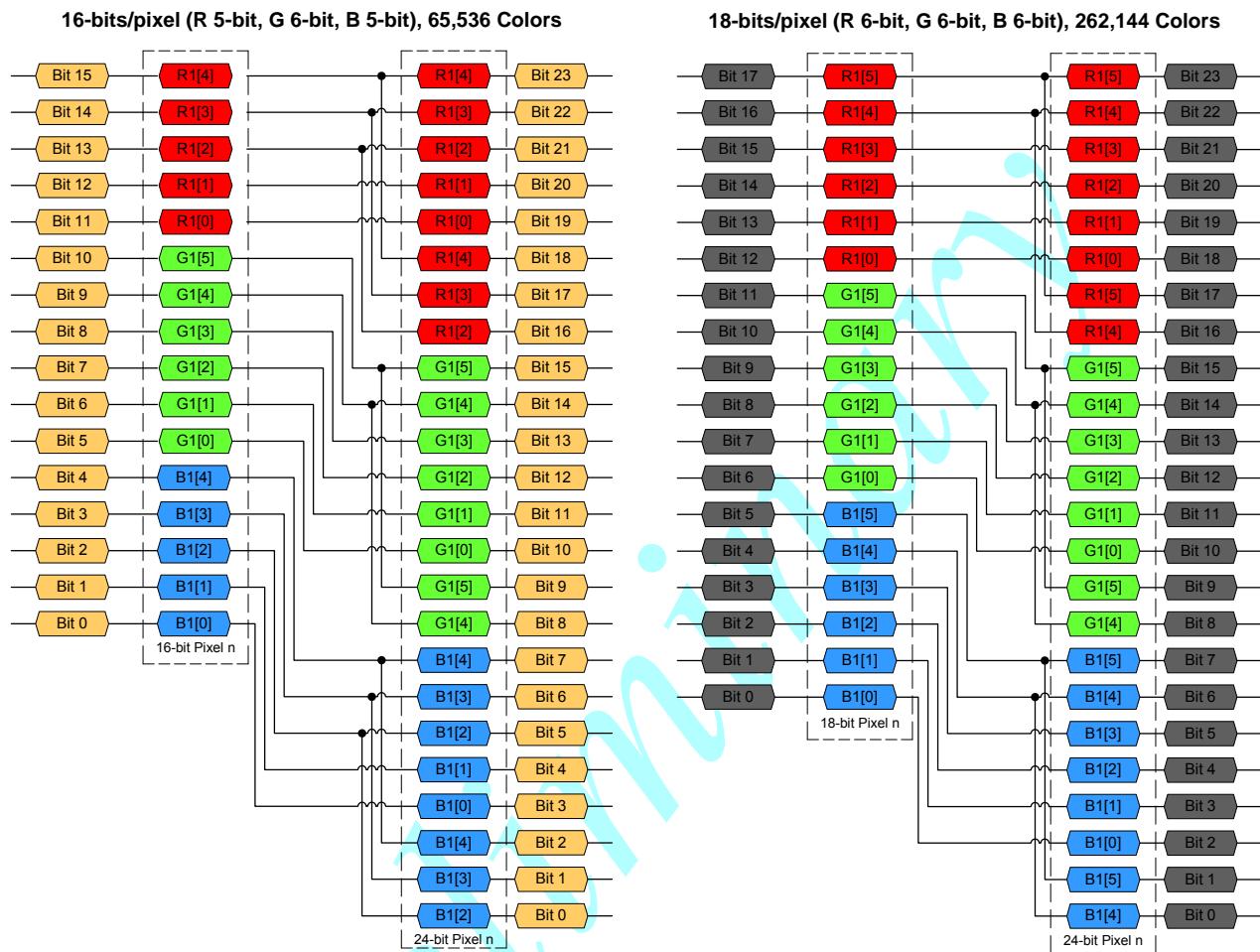


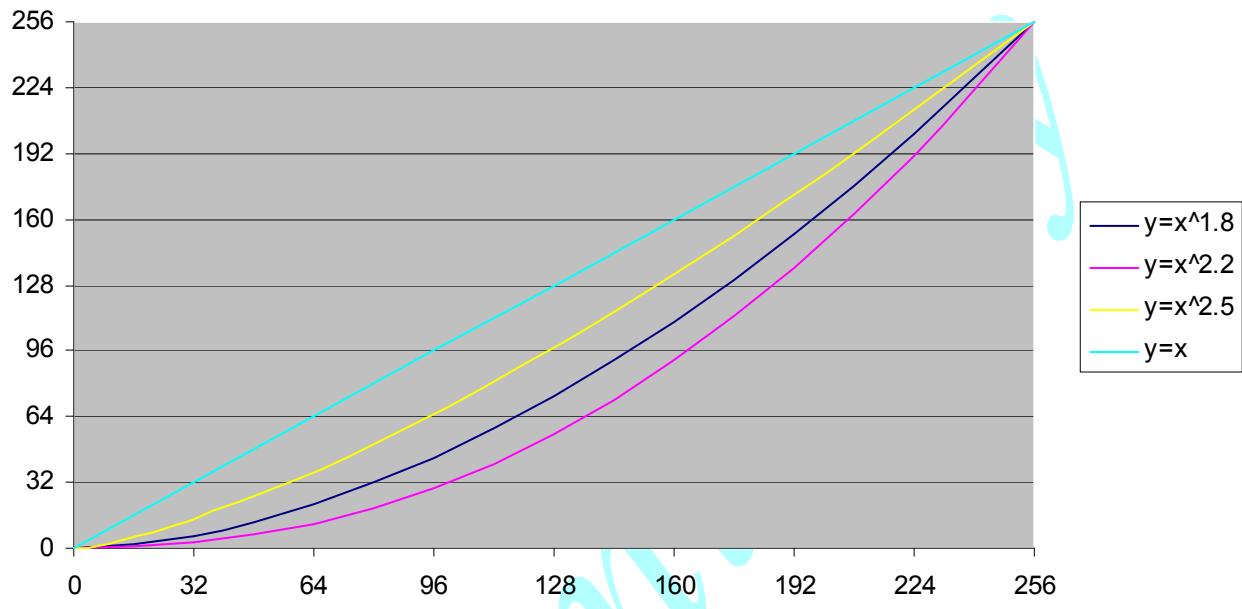
Table 6-8: 24-bit bus data formats (continued)



### 6.3 Gamma

The Gamma table is used to provide the power-law correction needed to accurately reproduce the desired color on the display. The DA8620 supports 4 standard gamma curves as shown in Figure 6-17.

**Figure 6-17: Gamma Curve Example**



The active gamma curve is selected with the GAMSET (0x26) register (see section 9.20). The default curve is  $y=OTP_1$ . Gamma correction is applied to the pixel data before it is written to the RAM and the "No Gamma Curve Selected" option is provided to bypass any gamma correction and guarantee that what is read out is what is written in.

**Table 6-9: Gamma Control Register**

Address	OTP	Name	Type	Bit Values								Initial Value					
				b7	b6	b5	b4	B3	b2	b1	b0						
0x26	Yes	GAMSET (Set Gamma Curve)	W	0	0	0	0	GAMMA				0x01					
				GAMMA:													
				0000	No Gamma Curve Selected												
				0001	GC0: $y = OTP_1$												
				0010	GC1: $y = OTP_2$												
				0100	GC2: $y = OTP_3$												
				1000	GC3: $y = OTP_4$												

Note:  $OTP_1$  to  $OTP_4$  are factory-programmable Gamma curves

### 6.4 Brightness Adjust

Please refer to the Brightness Adjust Application Note

## 7: Power Considerations

### 7.1 Power Modes

Five non-mutually exclusive power modes are supported: (A) Normal Mode; (B) Partial Mode; (C) Idle Mode; (D) Sleep Mode, and (E) Power OFF mode, which together give six distinct power level states.

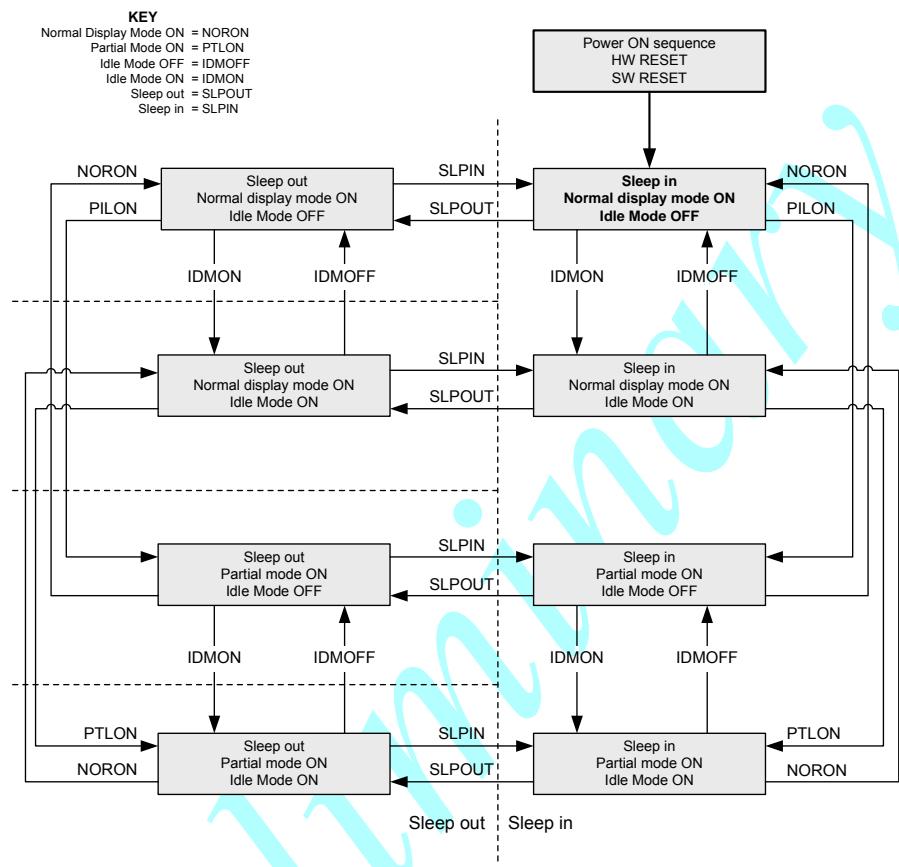
These states are listed below, in order of descending power consumption:

1. Normal Mode ON (full display), Idle Mode OFF, Sleep OUT.  
In this mode, the display is able to show maximum 16,777,216 colors across all 320 rows of the display.
2. Partial Mode ON, Idle Mode OFF, Sleep OUT.  
In this mode part of the display is used with maximum 16,777,216 colors.
3. Normal Mode ON (full display), Idle Mode ON, Sleep OUT.  
In this mode, the full display area is used but with replicated, averaged, or reduced 8 colors.
4. Partial Mode ON, Idle Mode ON, Sleep OUT.  
In this mode, part of the display is used with replicated, averaged, or reduced 8 colors.
5. Sleep IN Mode.  
In this mode, internal oscillator and panel driver circuit are stopped. Only the MPU interface and memory are active with VDDI power supply. Contents of the memory are safe. The oscillator must be manually started (Register 0xB2 Oscillator ON command - see section 9.39) before the RAM can be accessed. Note the DC:DC is an external circuit and could be active in this mode.
6. Power OFF Mode.  
In this mode, the internal 1.5 V LDO (digital supply) is turned off, along with the internal bias and Bandgap circuit. The device interface is not active and all RAM contents are lost.

Note: Transitions between states 1 to 5 are controllable by MCU commands. State 6 is entered only when the PWROFF command (0xB4) is given or the VDD power supply is removed. The state transition diagram is shown below in Figure 7-1:

## **Preliminary Data Sheet. Version 2b**

**Figure 7-1: Power States**



## **Power Mode A - Normal Mode**

Normal mode is defined by the absence of any other power mode, with the display turned ON. The Normal Mode ON command (0x13) is used to place the device in the normal mode.

#### **Power Mode B - Partial Mode**

The Partial Mode ON command (0x12) puts the device in to the partial area mode. The starting scan line and duty ratio are then defined by the contents of the partial area register (0x30). Neither the display refresh rate, nor the contents of the Main RAM, are effected by this command - it simply masks the data that is outside the partial area. If the content of the screen outside the defined partial area is already black, then entering partial mode will have no visible effect on either the display or power consumption.

### **Power Mode C - Idle Mode**

The Idle Mode ON command (0x39) puts the device into the low color/resolution idle mode. The default operation is to reduce the colors to 8-bits per pixel.

#### **Power Mode D - Sleep-IN Mode**

The Sleep-IN command (0x10) puts the device into the low-power sleep mode. The following conditions then apply:

- The Display turns OFF (Anodes connected to VL, Cathodes to VSSDISPLAY)
  - The Oscillator stops
  - The Display Internal bias / cascode voltage generator and reverse bias regulators are turned OFF
  - The control register contents and RAM data are preserved.

When exiting Sleep Mode, the oscillator is restarted, but the display remains in the defined state. The interface is fully functional in the Sleep Mode, and Control Register data can be transferred. The RAM is not accessible unless the

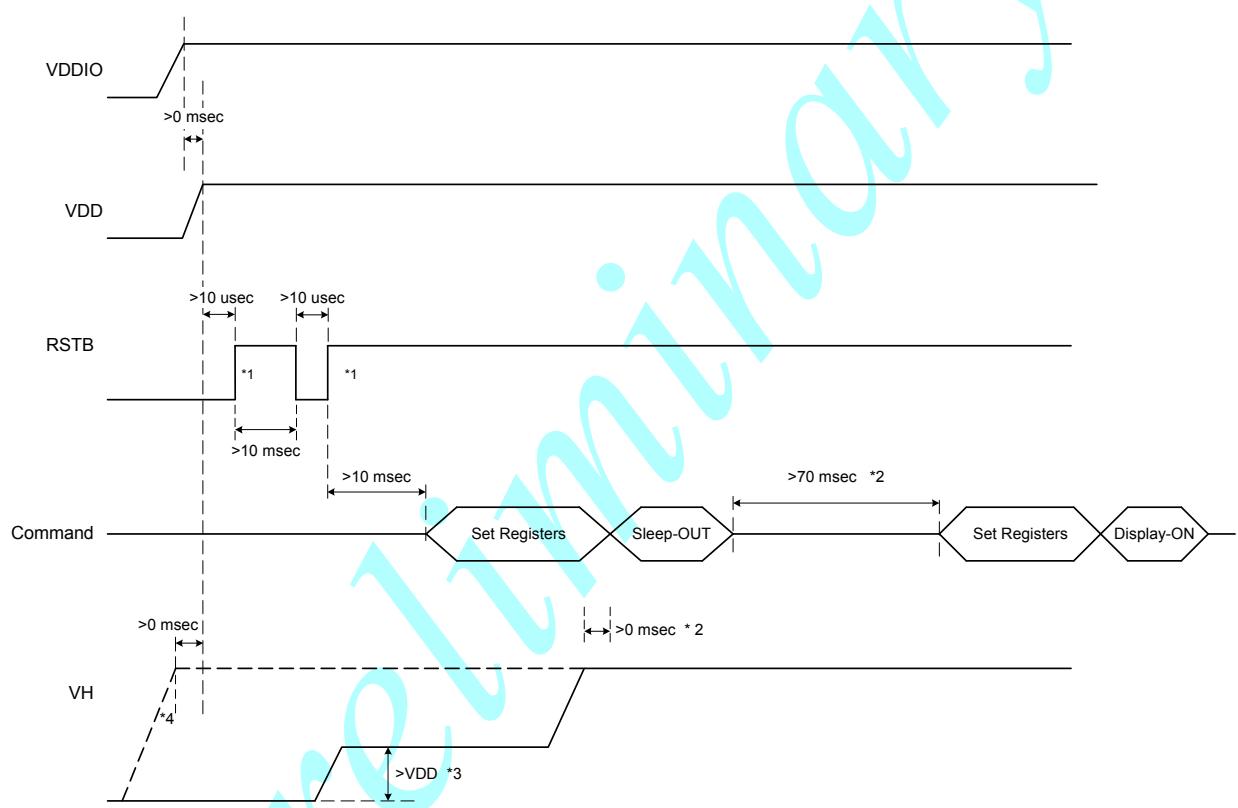
oscillator is manually started (OSCON command, register 0xB2 on page 126). The internal bias, bandgap and 1.5 V LDO are all active in SLEEP MODE.

#### Power Mode E - Power OFF Mode

The device enters the Power OFF mode when a PWROFF (0xB4) command is issued. In this mode the internal bias, bandgap and 1.5 V (DVDD supply) are all switched off. To exit this mode a low-to-high transition on RSTB pin must be made (this transition is not filtered). This will enable the internal power supply for the digital circuitry.

## 7.2 Power sequence diagrams

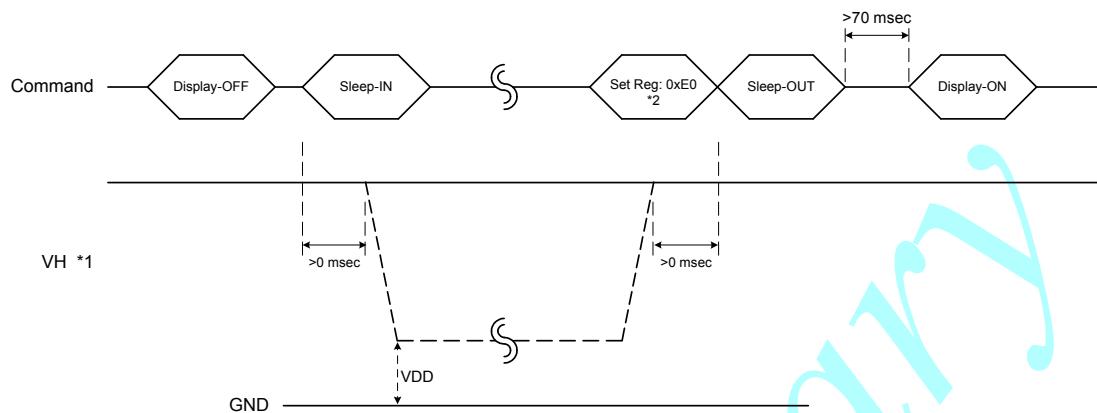
Figure 7-2: Power-ON sequence



#### Notes

- \*1. The first RSTB rising edge enables the DVDD LDO (i.e. it generates the power supply for the digital block), if it has not already started with application of VDD. The second one runs the Boot sequence.
- \*2. Anode calibration starts after sleep-out. Therefore VH should be allowed to settle before the sleep-out command is issued.  
Note: No register changes will be accepted during anode calibration.
- \*3. VH must be above VDD while VDD is ON.
- \*4. VH can be supplied before VDD.

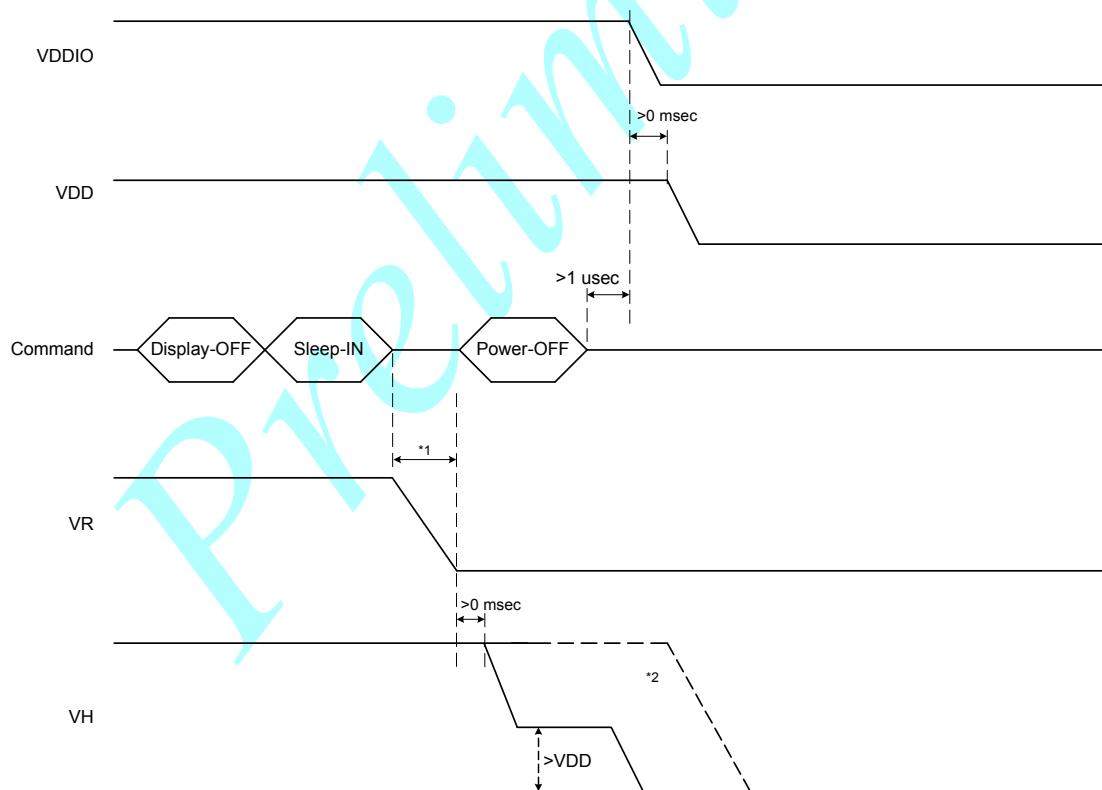
Figure 7-3: Sleep-IN/OUT sequence



## Notes

- \*1 It is acceptable to reduce VH to VDD (VH > VDD). However, this action will delete anode calibration data.
- \*2 If Reg:0xE0 is programmed in OTP, there is no need to set Reg: 0xE0. It is possible to set Reg: 0xE0 just before Display-ON.

Figure 7-4: Power-OFF sequence



## Notes

- \*1. Power-OFF should be issued after VR = 0. The time depends on the VR voltage and the decoupling capacitor value on VR.
- \*2. VH must turn off after VR = 0. VH must be above VDD while VDD is ON. e.g. VH can be set to battery voltage during power off.

### 7.3 Sequencer

The sequencer is responsible for handling the power-mode transition sequencing. The device power modes are described in the functional description (Power modes). Transitions between power modes are triggered by standard MIPI DCS commands as shown in Figure 7-1. The actions can be summarized as:

**Table 7-1: State Transition Actions**

Transition	Action
No-Power → Sleep-In	Enable LDO Start OSC Load values from OTP, includes repairing RAM Initialize RAM to zero Stop OSC
Sleep-In → Sleep-Out	Start OSC Reload values from OTP (perform Register Loading Detection and Functionality detection)
Sleep-Out → Sleep-Out (receive SLPOUT command)	Reload values from OTP (perform Register Loading Detection and Functionality detection)
Sleep-Out → Sleep-In	Display turns off Stop OSC Turn off display internal bias, cascade voltage generator, and reverse bias regulator
Any → No-Power	Turn off internal bias, bandgap, and 1.5 V DVDD supply

### 7.4 Headroom Detect and Booster Control IDAC

Please refer to the Headroom Detect and Booster Control IDAC application note.

### 7.5 Anode

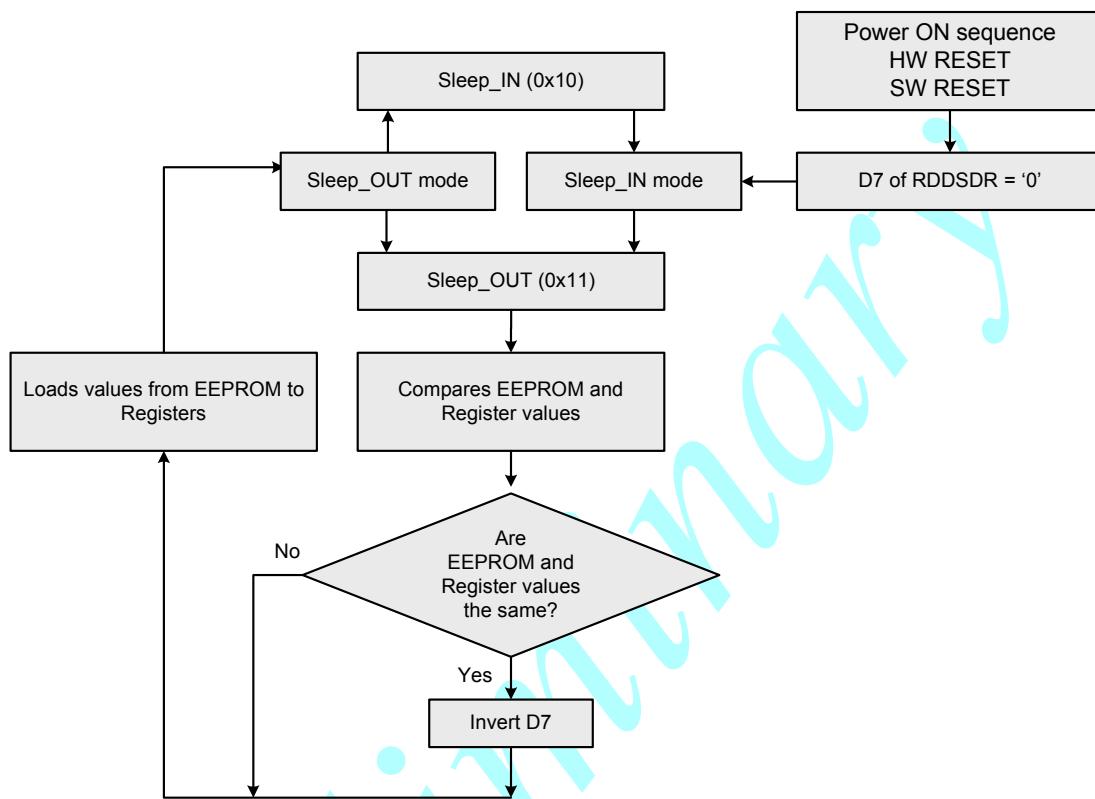
The anodes generate the current for driving the OLEDs: these currents are pulse width modulated. Each Anode current source is an 8-bit DAC, able to support 16 M colors. The minimum current is 0  $\mu$ A, and the maximum is 133  $\mu$ A.

### 7.6 Self-Diagnostic Functions

#### 7.6.1 Register Loading Detection

The SLPOUT command (0x11) is a trigger for the Register Loading Detection function. This function indicates if the display module correctly loaded the factory default values from Non-volatile memory to the registers. If the registers were loaded properly then bit D7 of the SDR register - read using the RDDSRR (0x0F) command - is inverted, otherwise the value is unchanged.

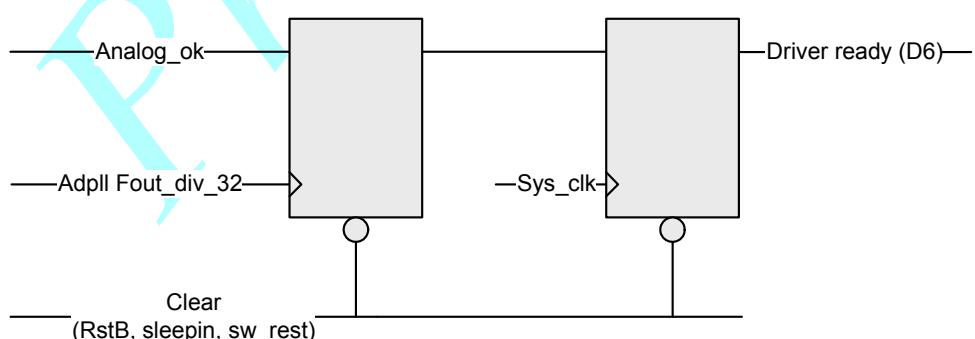
Figure 7-5: Flow Chart for Register Loading Detection



### 7.6.2 Functionality Detection

The SLPOUT command (0x11) is a trigger for the Functionality Detection function. This function indicates if the display module functional blocks, e.g. power supply, clock generator, etc. are operating correctly. If the functional blocks are operating properly then bit D6 of the SDR register - read using the RDDSRR (0x0F) command - is inverted, otherwise the value is unchanged.

Figure 7-6: Functionality Detect Circuit



## 8: Control Register Summary

The DA8620 is configured and controlled by writing or reading a bank of internal addressable control registers. The user must ensure that the control registers are correctly configured before display operation is started.

The Display Command Set (DCS) is used to store image data, configure the display module behavior and retrieve display module data including identification information by accessing the frame memory and the display module registers.

The DCS is separated into two functional areas: the User Command Set and the Manufacturer Command Set. Each command is an eight-bit code with 0x00 to 0xAF assigned to the User Command Set and all other codes assigned to the Manufacturer Command Set.

The User Command Set (UCS) provides a display device-independent interface targeted at the hardware abstraction layer of the operating system. Any unused command codes are treated as NOP by the display module.

The Manufacturer Command Set (MCS) is a device-dependent interface intended for factory programming of the display module default parameters. Once the display module has been configured, the MCS is disabled by the manufacturer. Once disabled, all MCS commands are treated as NOP by the display interface.

In the parallel MPU modes all reads automatically have a dummy byte as the first returned value (see Chapter 5 on page 25). In the serial MPU modes there are no dummy clocks. All register descriptions below have the dummy omitted.

### 8.1 Register Summary

#### Key:

Color	Meaning
Light Green	MIPI DCS (fields in <b>bold red</b> will return zero in this mode)
Light Blue	Nokia NDMIF
Light Orange	Dialog-specific
Light Grey	Unused

Note1: Unless explicitly named, register bits default to D[7:0] in the descriptions.

Note2: fields in **bold red** will return zero when the MIPI DCS mode is selected.

### 8.1.1 User Command Set

**Table 8-1: Register Map (Sheet 1 of 7)**

Address	OTP?	Name	R/W?	Bit values								Initial value
				D7	D6	D5	D4	D3	D2	D1	D0	
0x00	No	NOP (No Operation)	C	---	---	---	---	---	---	---	---	0x00
0x01	No	SWRESET (Software Reset)	C	---	---	---	---	---	---	---	---	0x00
0x02												
0x03												
0x04	Yes	RDDIDIF (Read Display Identification Info)	R	Manufacturer ID								0x00
				Type and Version								0x00
				Display Module								0x00
0x05		Not Implemented – Read Number of Parity Errors										
0x06	No	RDRED (Read Red Color)	R	R7	R6	R5	R4	R3	R2	R1	R0	N/A
				where: 8 bpp: R2 = MSB, R0 = LSB. R[7:3] = 0 12 bpp: R3 = MSB, R0 = LSB. R[7:4] = 0 16 bpp: R5 = MSB, R1 = LSB. R7, R6, R0 = 0 18 bpp: R5 = MSB, R0 = LSB. R7 and R6 = 0 24 bpp: R7 = MSB, R0 = LSB. All bits are used								
0x07	No	RDGREEN (Read Green Color)	R	G7	G6	G5	G4	G3	G2	G1	G0	N/A
				where: 8 bpp: G2 = MSB, G0 = LSB. G[7:3] = 0 12 bpp: G3 = MSB, G0 = LSB. G[7:4] = 0 16 bpp: G5 = MSB, G0 = LSB. G7 and G6 = 0 18 bpp: G5 = MSB, G0 = LSB. G7 and G6 = 0 24 bpp: G7 = MSB, G0 = LSB. All bits are used								
0x08	No	RDBLUE (Read Blue Color)	R	B7	B6	B5	B4	B3	B2	B1	B0	N/A
				where: 8 bpp: B1 = MSB, B0 = LSB. B[7:2] = 0 12 bpp: B3 = MSB, B0 = LSB. B[7:4] = 0 16 bpp: B5 = MSB, B1 = LSB. B7, B6, B0 = 0 18 bpp: B5 = MSB, B0 = LSB. B7 and B6 = 0 24 bpp: B7 = MSB, B0 = LSB. All bits are used								

P1

Table 8-1: Register Map (Sheet 2 of 7)

Address	OTP?	Name	R/W?	Bit values								Initial value	
				D7	D6	D5	D4	D3	D2	D1	D0		
0x09	No	RDDST (Read Display Status)	R	0	D30	D29	D28	D27	D26	0	0	N/A	
				0	1	1	1	D19	D18	D17	D16		
				0	0	D13	D12	D11	D10	D9	D8		
				D7	D6	D5	D4	D3	D2	D1	0		
				where:									
				D31	Reserved (Booster Voltage)								
				D30	Page Address Order								
				D29	Column Address Order								
				D28	Page/Column Order								
				D27	Vertical Order (Cathodes)								
				D26	RGB/BGR Order								
				D25	Reserved (Horizontal Order)								
				D24	Reserved (Segment Outputs)								
				D23	Reserved (Common Outputs)								
				D22	Pixel Format N/A as multiple interfaces								
				D21	“ “								
				D20	“ “								
				D19	Idle Mode On/Off								
				D18	Partial Mode On/Off								
				D17	Sleep In/Out								
				D16	Display Normal Mode On/Off								
				D15	Reserved (Vertical Scroll)								
				D14	Reserved (Horizontal Scroll)								
				D13	Inversion Status								
				D12	All Pixels On								
				D11	All Pixels Off								
				D10	Display On/Off								
				D9	Tearing Effect Line On/Off								
				D8	Gamma Curve Selection								
				D7	“ “								
				D6	“ “								
				D5	Tearing Effect Output Line Mode								
				D4	Horizontal Sync (new slice)								
				D3	Vertical Sync (Rsync)								
				D2	Pixel Clock								
				D1	Data Enable								
				D0	Reserved (Parity Error on CDP)								
0x0A	No	RDDPM (Read Display Power Mode)	R	0	D6	D5	D4	D3	D2	0	0	N/A	
				where:									
				D7	Reserved								
				D6	Idle Mode On/Off								
				D5	Partial Mode On/Off								
				D4	Sleep Mode On/Off								
				D3	Normal Mode On/Off								
				D2	Display On/Off								
				D1	Reserved								
				D0	Reserved								

Table 8-1: Register Map (Sheet 3 of 7)

Address	OTP?	Name	R/W?	Bit values								Initial value					
				D7	D6	D5	D4	D3	D2	D1	D0						
0x0B	No	RDDMADCTL (Read Display Memory Access Control)	R	D7	D6	D5	D4	D3	0	0	0	N/A					
				where:													
				D7	Page Address Order												
				D6	Column Address Order												
				D5	Page/Column Order												
				D4	Vertical Order (Cathodes)												
				D3	RGB/BGR Order												
				D2	Reserved (Horizontal Order)												
				D1	Reserved (Segment Outputs)												
				D0	Reserved (Common Outputs)												
0x0C	No	RDDCOLMOD (Read Display Pixel Format)	R	0	RGBPF		0	MPUPF				0x67					
				where: xxxPF is given by the following table:													
				000	Reserved												
				001	Reserved												
				010	8 bits/pixel												
				011	12 bits/pixel												
				100	Reserved												
				101	16 bits/pixel												
				110	18 bits/pixel												
				111	24 bits/pixel												
0x0D	No	RDDIM (Read Display Image Mode)	R	0	0	D5	<b>D4</b>	<b>D3</b>	GAMMA				N/A				
				where:													
				D7	Reserved (Vertical Scroll)												
				D6	Reserved (Horizontal Scroll)												
				D5	Inversion Status												
				D4	All Pixels On												
				D3	All Pixels Off												
				GAMMA:													
				000	GC0: y = OTP <sub>1</sub> (default)												
				001	GC1: y = OTP <sub>2</sub>												
0x0E	No	RDDSM (Read Display Signal Mode)	R	010	GC2: y = OTP <sub>3</sub>							N/A					
				011	GC3: y = OTP <sub>4</sub>												
				D7	D6	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	0	0						
				where:													
				D7	Tearing Effect Line On/Off												
				D6	Tearing Effect Output Line Mode												
				D5	Horizontal Sync (new slice)												
0x0F	No	RDDSDR (Read Display Self-Diagnostic Result)	R	D4	Vertical Sync (Rsync)							N/A					
				D3	Pixel Clock												
				D2	Data Enable												
				D7	D6	D5	D4	0	0	0	0						
				where:													
				D7	Register Loading Detection												
				D6	Functionality Detection												
				D5	Chip Attachment Detection												
				D4	Display Glass Break Detection												

Table 8-1: Register Map (Sheet 4 of 7)

Address	OTP?	Name	R/W?	Bit values								Initial value					
				D7	D6	D5	D4	D3	D2	D1	D0						
Address	OTP	Name	Type	Bit Values								Initial Value					
				b7	B6	b5	b4	b3	b2	b1	b0						
0x0B	No	RDDMADCTL (Read Display Memory Access Control)	R	D7	D6	D5	D4	D3	0	0	0	N/A					
				where:													
				D7	Page Address Order												
				D6	Column Address Order												
				D5	Page/Column Order												
				D4	Vertical Order (Cathodes)												
				D3	RGB/BGR Order												
				D2	Reserved (Horizontal Order)												
				D1	Reserved (Segment Outputs)												
				D0	Reserved (Common Outputs)												
0x0C	No	RDDCOLMOD (Read Display Pixel Format)	R	0	RGBPF		0	MPUPF				0x67					
				where: xxxPF is given by the following table:													
				000	Reserved												
				001	Reserved												
				010	8	bits/pixel											
				011	12	bits/pixel											
				100	Reserved												
				101	16	bits/pixel											
				110	18	bits/pixel											
				111	24	bits/pixel											
0x0D	No	RDDIM (Read Display Image Mode)	R	0	0	D5	D4	D3	GAMMA				N/A				
				where:													
				D7	Reserved (Vertical Scroll)												
				D6	Reserved (Horizontal Scroll)												
				D5	Inversion Status												
				D4	All Pixels On												
				D3	All Pixels Off												
				GAMMA:													
				000	GC0: y = x^2.2	(default)											
				001	GC1: y = x^1.8												
0x0E	No	RDDSM (Read Display Signal Mode)	R	010	GC2: y = x^2.5												
				011	GC3: y = x												
				D7	D6	D5	D4	D3	D2	0	0	N/A					
				where:													
				D7	Tearing Effect Line On/Off												
				D6	Tearing Effect Output Line Mode												
				D5	Horizontal Sync (new slice)												
				D4	Vertical Sync (Rsync)												
				D3	Pixel Clock												
				D2	Data Enable												

Table 8-1: Register Map (Sheet 5 of 7)

Address	OTP?	Name	R/W?	Bit values								Initial value	
				D7	D6	D5	D4	D3	D2	D1	D0		
0x0F	No	RDDSDR (Read Display Self-Diagnostic Result)	R	D7	D6	D5	D4	0	0	0	0	N/A	
				where:									
				D7	Register Loading Detection								
				D6	Functionality Detection								
				D5	Chip Attachment Detection								
				D4	Display Glass Break Detection								
0x10	No	SLPIN (Sleep In)	C	---								0x00	
0x11	No	SLPOUT (Sleep Out)	C	---								0x00	
0x12	No	PTLON (Partial Mode On)	C	---								0x00	
0x13	No	NORON (Normal Mode On)	C	---								0x00	
14 ... 0x1F		Reserved											
0x20	No	INVMOFF (Inversion Mode Off)	C	---								0x00	
0x21	No	INVMON (Inversion Mode On)	C	---								0x00	
0x22	No	ALLPIXOFF (All Pixels Off)	C	---								0x00	
0x23	No	ALLPIXON (All Pixels On)	C	---								0x00	
0x24 ... 0x25													
0x26	Yes	GAMSET (Set Gamma Curve)	W	GC[7:0]								0x01	
				GC[7:0]:									
				0x00	No Gamma Curve Selected								
				0x01	GC0: $y = x^{2.2}$								
				0x02	GC1: $y = x^{1.8}$								
				0x04	GC2: $y = x^{2.5}$								
				0x08	GC3: $y = x$								
0x27													
0x28	No	DISPOFF (Display Off)	C	---								0x00	
0x29	No	DISPON (Display On)	C	---								0x00	
0x2A	Yes	CASET (Column Address Set)	W	0	0	0	0	0	0	SC[9:8]		0x00 0x00 0x00 0xEF	
				SC[7:0]									
				0	0	0	0	0	0	EC[9:8]			
				EC[7:0]									
0x2B	Yes	PASET (Page Address Set)	W	0	0	0	0	0	0	SP[9:8]		0x00 0x00 0x01 0x3F	
				SP[7:0]									
				0	0	0	0	0	0	EP[9:8]			
				EP[7:0]									
0x2C	No	RAMWR (Write Memory Start)	W	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									
0x2D		Not Implemented – Write LUT											
0x2E	No	RAMRD (Read Memory Start)	R	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									
0x2F													

Table 8-1: Register Map (Sheet 6 of 7)

Address	OTP?	Name	R/W?	Bit values								Initial value					
				D7	D6	D5	D4	D3	D2	D1	D0						
0x30	No	PTLAR (Partial Area)	W	0	0	0	0	0	0	SR[9:8]		0x00					
				SR[7:0]								0x00					
				0	0	0	0	0	0	ER[9:8]		0x00					
				ER[7:0]								0x00					
0x31 ... 0x32																	
0x33		Not Implemented – Vertical Scrolling Area															
0x34	No	TEOFF (Tearing Effect Line Off)	C	---								0x00					
0x35	No	TEON (Tearing Effect Line On)	C	0	0	0	0	0	0	0	M	0x00					
				where:													
				M	Tearing Effect Mode												
0x36	Yes	MADCTL (Memory Access Control)	W	D7	D6	D5	D4	D3	0	0	0	0x00					
				where:													
				D7	Page Address Order												
				D6	Column Address Order												
				D5	Page/Column Order												
				D4	Vertical Order (Cathodes)												
0x37		Not Implemented – Vertical Scrolling Start Address		D3													
				RGB/BGR Order													
0x38	No	IDMOFF (Idle Mode Off)	C	---								0x00					
0x39	No	IDMON (Idle Mode On)	C	---								0x00					
0x3A	Yes	COLMOD (Set Display Pixel Format)	W	0	RGBPF		0	MPUPF				0x67					
				where: xxxPF is given by the following table:													
				000	Reserved												
				001	Reserved												
				010	8 bits/pixel												
				011	12 bits/pixel												
				100	Reserved												
				101	16 bits/pixel												
				110	18 bits/pixel												
				111	24 bits/pixel												
0x3B																	
0x3C	No	RAMWRC (Memory Write Continue)		1 <sup>st</sup> Parameter													
				2 <sup>nd</sup> Parameter													
				...													
				Last Parameter													
0x3D																	
0x3E	No	RAMRDC (Memory Read Continue)		1 <sup>st</sup> Parameter													
				2 <sup>nd</sup> Parameter													
				...													
				Last Parameter													
0x3F																	
0x40 ... 0x43																	
0x44	Yes	TESLSET (Tear Scan line Set)	W	0	0	0	0	0	0	N[9:8]		0x00					
				N[7:0]								0x00					

**Table 8-1: Register Map (Sheet 7 of 7)**

Address	OTP?	Name	R/W?	Bit values								Initial value	
				D7	D6	D5	D4	D3	D2	D1	D0		
0x45	No	CURSL (Current Scan line)	R	0	0	0	0	0	0	N[9:8]	N/A		
0x46 ... 0x4F				N[7:0]									
0x50 ... 0x5F													
0x60 ... 0x6F													
0x70 ... 0x7F													
0x80 ... 0x8F													
0x90 ... 0x9F													
0xA0													
0xA1	Yes	RDDDB (Read DDB Start)	R	1 <sup>st</sup> Parameter								0xFF	
				2 <sup>nd</sup> Parameter								0xFF	
				...								...	
				Last Parameter								0xFF	
0xA2 ... 0xAF													

### 8.1.2 Manufacturer Command Set

These registers provide some key functionalities not defined yet in the standard MIPI Display Command Set and occupy the address space 0xB0<sub>H</sub> to 0xBF.

**Table 8-2: Manufacturer Base Control Registers**

Address	OTP?	Name	R/W?	Bit values								Initial value			
				D7	D6	D5	D4	D3	D2	D1	D0				
0xB0		Reserved													
0xB1		Reserved													
0xB2	No	OSCON (Oscillator On)	C	---								0x00			
0xB3	No	OSCOFF (Oscillator Off)	C	---								0x00			
0xB4	No	PWROFF (Power Off)	C	---								0x00			
0xB5	No	DIMSET (Dimmer Set)	C	0	0	0	0	0	0	DIM		0x00			
				DIM:											
				00	Normal Mode										
				01	1/2 Brightness										
				10	1/4 Brightness										
				11	1/8 Brightness										
0xB6		Reserved	C												
0xB7		Reserved	C												
0xB8		Reserved	R												
0xB9	No	BRIGHTLM (Brightness Level Monitor)		Please refer to Application Note											
0xBA		BRIGHTSET (Brightness Set)		Please refer to Application Note											
0xBB	Yes	BWCONV (Black & white convert)	W	Multiplier for Red								0x4D			
				Multiplier for Green								0x97			
				Multiplier for Blue								0x1C			
0xBC ... 0xBF		Reserved													

### 8.1.3 Interface Control Registers

The Interface control registers define the polarity of the input signals and define the windowing scheme. These registers occupy the address space 0xC0 to 0xC7.

**Table 8-3: Interface Control Registers**

Address	OTP?	Name	R/W?	Bit values								Initial value
				D7	D6	D5	D4	D3	D2	D1	D0	
0xC0	Yes	DCSCTL (DCS Control)	W	BW	BM	CS	CH	TE	SG	RGBOPT	MPUOPT	0x10
				0	0	0	0	0	0	0	0	0x00
0xC1	Yes	RGBCTL (RGB Control)	W	D7	D6	D5	D4	D3	D2	MODE		0x01
0xC2	Yes	SERID (Serial Interface ID)	W	0	0	Slave Address						
0xC3		Reserved										
0xC4		Reserved										
0xC5		Reserved										
0xC6		Reserved										
C7~0xCF		Reserved										

### 8.1.4 Miscellaneous Registers

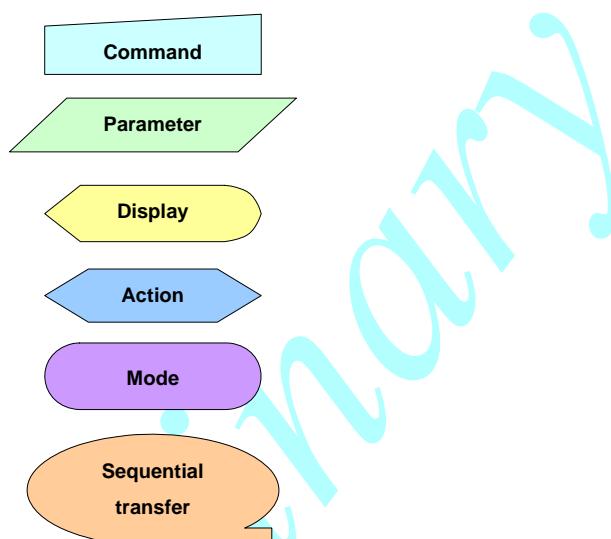
**Table 8-4: Interface Control Registers**

Address	OTP?	Name	R/W?	Bit values								Initial value
				D7	D6	D5	D4	D3	D2	D1	D0	
0xDA	No	RDID1	R	Manufacturer ID								0XX
0xDB	No	RDID2	R	Type and Version								0YY
0xDC	No	RDID3	R	Display Module								0ZZ
0xE0		ANCTLSET (Set Analog Control)		Refer to application note								
0xE1~0xEF		Reserved		Reserved								

## 9: Register Details

**Note:** In all register flowcharts, the shapes and colors of the elements are defined as follows:

Figure 9-1: Flowchart Shape Definitions



### 9.1 0x00 No Operation (NOP)

Table 9-1: 0x00 No Operation Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x00	No	NOP (No Operation)	C	..	..	..	..	..	..	..	..	0x00

This command is an empty command; it does not have any effect on the display module. However, it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write), RAMWRC (Memory Write Continue), RAMRD (Memory Read), and RAMRDC (Memory Read Continue) Commands.

#### Restrictions

None.

#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

#### Flow Chart

None.

## 9.2 0x01 Software Reset

**Table 9-2: 0x01 Software Reset Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x01	No	Software Reset	C	...								0x00

When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values (See default tables in each command description).

The Frame Memory contents are unaffected by this command.

### Restrictions

The host processor must wait five milliseconds before sending any new commands to a display module following this command. The display module updates the registers during this time.

If a SWRESET is sent when the display module is in Sleep Mode, the host processor must wait 120 milliseconds before sending an SLPOUT (0x11) command.

SWRESET should not be sent when the display module is not in Sleep mode.

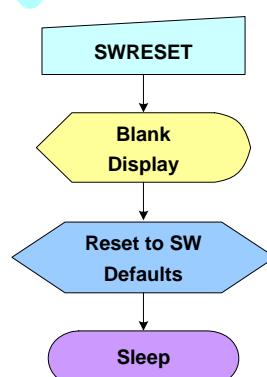
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

### Flow Chart



### 9.3 Read Display Identification Info – RDDIDIF (0x04)

#### Bit Definitions

Table 9-3: 0x04 Read Display Identification Info Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x04	Yes	RDDIDIF (Read Display Identification Info)	R	Manufacturer ID								0XX
				Type and Version								0YY
				Display Module								0ZZ

#### Description

This read command returns the 24-bit display identification information. The data returned is the same as that returned by the RDID1 (0xDA), RDID2 (0xDB), and RDID3 (0xDC) commands.

#### Restrictions

None.

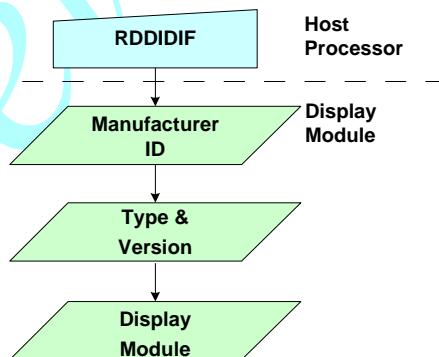
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

#### Flow Chart



## 9.4 0x05 to 0x07 Read Color Registers

### 9.4.1 Read Red

#### Bit Definitions

**Table 9-4: Read Red Color – RDRED (0x06) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x06	No	RDRED (Read Red Color)	R	R7	R6	R5	R4	R3	R2	R1	R0	N/A

where:  
 8 bpp: R2 = MSB, R0 = LSB. R[7:3] = 0  
 12 bpp: R3 = MSB, R0 = LSB. R[7:4] = 0  
 16 bpp: R5 = MSB, R1 = LSB. R7, R6, R0 = 0  
 18 bpp: R5 = MSB, R0 = LSB. R7 and R6 = 0  
 24 bpp: R7 = MSB, R0 = LSB. All bits are used

#### Description

The display module returns the red component value of the first pixel in the active frame. Only the relevant bits are used according to the pixel format; unused bits are set to '0'.

#### Restrictions

None.

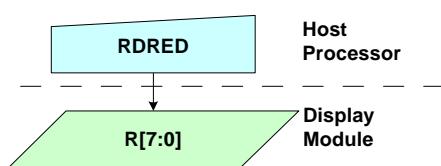
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

#### Flow Chart



### 9.4.2 Read Green

#### Bit Definitions

Table 9-5: Read Green Color – RDGREEN (0x07) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x07	No	RDGREEN (Read Green Color)	R	R7	R6	R5	R4	R3	R2	R1	R0	N/A
where:												
8 bpp: R2 = MSB, R0 = LSB. R[7:3] = 0												
12 bpp: R3 = MSB, R0 = LSB. R[7:4] = 0												
16 bpp: R5 = MSB, R1 = LSB. R7, R6, R0 = 0												
18 bpp: R5 = MSB, R0 = LSB. R7 and R6 = 0												
24 bpp: R7 = MSB, R0 = LSB. All bits are used												

#### Description

The display module returns the green component value of the first pixel in the active frame. Only the relevant bits are used according to the pixel format; unused bits are set to '0'.

#### Restrictions

None.

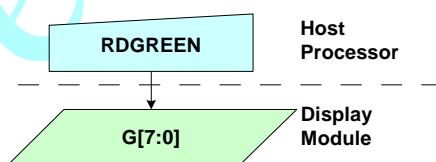
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

#### Flow Chart



### 9.4.3 Read Blue

#### Bit Definitions

Table 9-6: Read Blue Color – RDBLUE (0x08) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x08	No	RDBLUE (Read Blue Color)	R	R7	R6	R5	R4	R3	R2	R1	R0	N/A
where:												
8 bpp: R2 = MSB, R0 = LSB. R[7:3] = 0												
12 bpp: R3 = MSB, R0 = LSB. R[7:4] = 0												
16 bpp: R5 = MSB, R1 = LSB. R7, R6, R0 = 0												
18 bpp: R5 = MSB, R0 = LSB. R7 and R6 = 0												
24 bpp: R7 = MSB, R0 = LSB. All bits are used												

**Description**

The display module returns the blue component value of the first pixel in the active frame. Only the relevant bits are used according to the pixel format; unused bits are set to '0'.

**Restrictions**

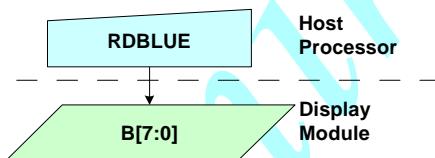
None.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

**Flow Chart**

## 9.5 Read Display Status – RDDST (0x09)

### Bit Definitions

Table 9-7: Read Display Status (0x09) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x09	No	RDDST (Read Display Status)	R	0	D30	D29	D28	D27	D26	0	0	N/A	
				0	1	1	1	D19	D18	D17	D16		
				0	0	D13	D12	D11	D10	D9	D8		
				D7	D6	D5	D4	D3	D2	D1	0		
				where:									
				D31	Reserved ( <i>Booster Voltage</i> )								
				D30	Page Address Order								
				D29	Column Address Order								
				D28	Page/Column Order								
				D27	Line Address Order (Cathodes)								
				D26	RGB/BGR Order								
				D25	Reserved ( <i>Horizontal Order</i> )								
				D24	Reserved ( <i>Segment Outputs</i> )								
				D23	Reserved ( <i>Common Outputs</i> )								
				D22	Pixel Format N/A as multiple interfaces								
				D21	“ “								
				D20	“ “								
				D19	Idle Mode ON/OFF								
				D18	Partial Mode ON/OFF								
				D17	Sleep In/Out								
				D16	Display Normal Mode ON/OFF								
				D15	Reserved ( <i>Vertical Scroll</i> )								
				D14	Reserved ( <i>Horizontal Scroll</i> )								
				D13	Inversion Status								
				D12	All Pixels ON								
				D11	All Pixels OFF								
				D10	Display ON/OFF								
				D9	Tearing Effect Line ON/OFF								
				D8	Gamma Curve Selection								
				D7	“ “								
				D6	“ “								
				D5	Tearing Effect Output Line Mode								
				D4	Horizontal Sync (new slice)								
				D3	Vertical Sync (Rsync)								
				D2	Pixel Clock								
				D1	Data Enable								
				D0	Reserved (Parity Error on CDP)								

### Description

The Read Display Status register contains the standard bit definitions as used by Nokia for returning basic display information. These Nokia bit definitions areas follows:

1. Bit D31 – Reserved (Booster Voltage)  
This is not used and should return '0'.
2. Bit D30 – Page Address Order  
'0' = Top to Bottom (When MADCTL B7 = '0').  
'1' = Bottom to Top (When MADCTL B7 = '1').
3. Bit D29 – Column Address Order  
'0' = Left to Right (When MADCTL B6 = '0').  
'1' = Right to Left (When MADCTL B6 = '1').
4. Bit D28 – Page/Column Order  
'0' = Normal Mode (When MADCTL B5 = '0').  
'1' = Reverse Mode (When MADCTL B5 = '1').
5. Bit D27 – Line Address Order  
'0' = OLED Refresh Top to Bottom (When MADCTL B4 = '0').  
'1' = OLED Refresh Bottom to Top (When MADCTL B4 = '1').
6. Bit D26 – RGB/BGR Order  
'0' = RGB (When MADCTL B3 = '0').  
'1' = BGR (When MADCTL B3 = '1').
7. Bit D25 – Reserved (Horizontal Order)  
This is unused and should return '0'.
8. Bit D24 – Reserved (Segment Outputs)  
This is unused and should return '0'.
9. Bit D23 – Reserved (Common Outputs)  
This is unused and should return '0'.
10. Bits D22, D21, D20 – Pixel Format  
As there are multiple interfaces, this will return '111'.
11. Bit D19 – Idle Mode ON/OFF  
'0' = Idle Mode OFF.  
'1' = Idle Mode ON.
12. Bit D18 – Partial Mode ON/OFF  
'0' = Partial Mode OFF.  
'1' = Partial Mode ON.
13. Bit D17 – Sleep In/Out  
'0' = Sleep Mode In/ON.  
'1' = Sleep Mode Out/OFF.
14. Bit D16 – Display Normal Mode ON/OFF  
'0' = Display Normal Mode OFF.  
'1' = Display Normal Mode ON.
15. Bit D15 – Reserved (Vertical Scrolling)  
This is unused and should return '0'.
16. Bit D14 – Reserved (Horizontal Scrolling)  
This is unused and should return '0'.
17. Bit D13 – Inversion ON/OFF  
'0' = Inversion OFF.  
'1' = Inversion ON.
18. Bit D12 – All Pixels ON  
'0' = All Pixels ON is not active.  
'1' = All Pixels ON.
19. Bit D11 – All Pixels OFF  
'0' = All Pixels OFF is not active.  
'1' = All Pixels OFF.

## 20. Bit D10 – Display ON/OFF

'0' = Display is OFF.

'1' = Display is ON.

## 21. Bit D9 – Tearing Effect Line ON/OFF

'0' = Tearing Effect Line OFF.

'1' = Tearing Effect Line ON.

## 22. Bits D8, D7, D6 – Gamma Curve Selection.

If no curve has been selected by GAMSET (0x26), then return '111' else return:

D8	D7	D6	Description
0	0	0	GC0: $y = OTP_1$
0	0	1	GC1: $y = OTP_2$
0	1	0	GC2: $y = OTP_3$
0	1	1	GC3: $y = OTP_4$
1	X	X	Not Defined

## 23. Bit D5 – Tearing Effect Line Output Mode

'0' = Mode 1, V-Blanking only.

'1' = Mode 2, both H-Blanking and V-Blanking.

## 24. Bit D4 – Horizontal Sync ON/OFF, Note 1

'0' = Horizontal Sync. bit/line is OFF ("Low").

'1' = Horizontal Sync. bit/line is ON ("High").

## 25. Bit D3 – Vertical Sync ON/OFF, Note 2

'0' = Vertical Sync. bit/line is OFF ("Low").

'1' = Vertical Sync. bit/line is ON ("High").

## 26. Bit D2 – Pixel Clock ON/OFF, Note 1

'0' = PCLK line is OFF ("Low").

'1' = PCLK line is ON ("High").

## 27. Bit D1 – Data Enable ON/OFF, Note 1

'0' = DE bit/line is OFF ("Low").

'1' = DE bit/line is ON ("High").

## 28. Bit D0 – Reserved (Parity Error on CDP)

This is not used and should return '0'.

Note: When the RGB mode is being used these signals represent the external signals presented to the interface when the command was received. In MPU mode they represent the internally generated equivalent signal.

**Restrictions**

None.

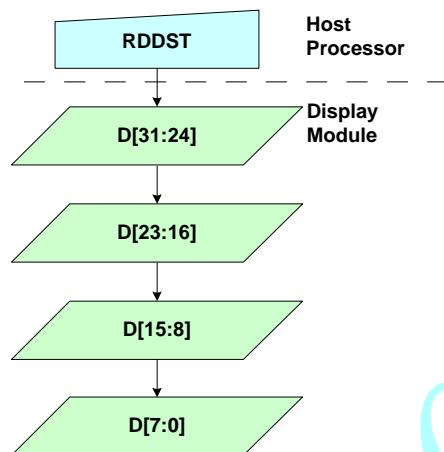
**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

## Flow Chart



## 9.6 Read Display Power Mode – RDDPM (0x0A)

## Bit Definitions

Table 9-8: Read Display Power Mode (0x0A) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x0A	No	RDDPM (Read Display Power Mode)	R	0	D6	D5	D4	D3	D2	0	0	N/A	
				where:									
				D7	Reserved								
				D6	Idle Mode On/Off								
				D5	Partial Mode On/Off								
				D4	Sleep Mode On/Off								
				D3	Normal Mode On/Off								
				D2	Display On/Off								
				D1	Reserved								
				D0	Reserved								

## Description

The Read Display Power Mode register returns the current power mode, as follows.

- Bit D7 – Reserved  
This is not used and should return '0'.
- Bit D6 – Idle Mode On/Off  
'0' = Idle Mode Off.  
'1' = Idle Mode On.
- Bit D5 – Partial Mode On/Off  
'0' = Partial Mode Off.  
'1' = Partial Mode On.
- Bit D4 – Sleep In/Out  
'0' = Sleep Mode In/On.  
'1' = Sleep Mode Out/Off.
- Bit D3 – Display Normal Mode On/Off  
'0' = Display Normal Mode Off.  
'1' = Display Normal Mode On.

- Bit D2 – Display On/Off  
 '0' = Display is Off.  
 '1' = Display is On.
- Bit D1 – Reserved  
 This is not used and should return '0'.
- Bit D0 – Reserved  
 This is not used and should return '0'.

#### Restrictions

None.

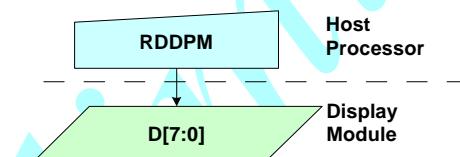
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	0x08
SW Reset	
HW Reset	

#### Flow Chart



## 9.7 Read Display Memory Access Control – RDDMACTL (0x0B)

#### Bit Definitions

Table 9-9: Read Display Memory Access Control (0x0B) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x0B	No	RDDMADCTL (Read Display Memory Access Control)	R	D7	D6	D5	D4	D3	0	0	0	N/A	
				where:									
				D7	Page Address Order								
				D6	Column Address Order								
				D5	Page/Column Order								
				D4	Vertical Order (Cathodes)								
				D3	RGB/BGR Order								
				D2	Reserved (Horizontal Order)								
				D1	Reserved (Segment Outputs)								
				D0	Reserved (Common Outputs)								

#### Description

The Read Display Memory Access Control returns the current display status as follows.

- Bit D7 – Page Address Order  
 '0' = Top to Bottom (When MADCTL B7 = '0').  
 '1' = Bottom to Top (When MADCTL B7 = '1').
- Bit D6 – Column Address Order  
 '0' = Left to Right (When MADCTL B6 = '0').  
 '1' = Right to Left (When MADCTL B6 = '1').
- Bit D5 – Page/Column Order  
 '0' = Normal Mode (When MADCTL B5 = '0').  
 '1' = Reverse Mode (When MADCTL B5 = '1').
- Bit D4 – Line Address Order  
 '0' = OLED Refresh Top to Bottom (When MADCTL B4 = '0').  
 '1' = OLED Refresh Bottom to Top (When MADCTL B4 = '1').
- Bit D3 – RGB/BGR Order  
 '0' = RGB (When MADCTL B3 = '0').  
 '1' = BGR (When MADCTL B3 = '1').
- Bit D2 – Reserved (Horizontal Order)  
 This is unused and should return '0'.
- Bit D1 – Reserved (Segment Outputs)  
 This is unused and should return '0'.
- Bit D0 – Reserved (Common Outputs)  
 This is unused and should return '0'.

#### Restrictions

None.

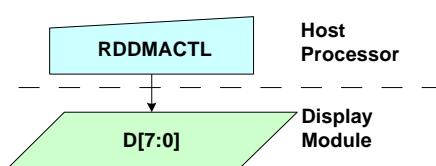
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	0x00
SW Reset	no change
HW Reset	0x00

#### Flow Chart



## 9.8 Read Display Pixel Format – RDDCOLMOD (0x0C)

### Bit Definitions

Table 9-10: Read Display Pixel Format (0x0C) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x0C	No	RDDCOLMOD (Read Display Pixel Format)	R	0	RGBPF			0	MPUPF			0x67

### Description

This command returns the pixel format for the RGB image data used by the interface.

- Bits D[6:4] – RGB Pixel Format Definition
- Bits D[2:0] – MPU Pixel Format Definition
- Bits D7 and D3 are not used and return ‘0’.

D6/ D2	D5/ D1	D4/ D0	Description
0	0	0	Reserved
0	0	1	Reserved
0	1	0	8 bits/pixel
0	1	1	12 bits/pixel
1	0	0	Reserved
1	0	1	16 bits/pixel
1	1	0	18 bits/pixel
1	1	1	24 bits/pixel

### Restrictions

None.

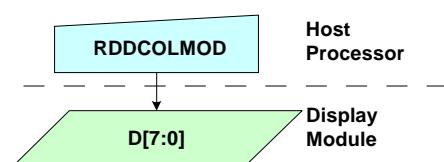
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power ON Sequence	0x67
SW Reset	0x67
HW Reset	0x67

### Flow Chart



## 9.9 Read Display Image Mode – RDDIM (0x0D)

### Bit Definitions

Table 9-11: Read Display Image Mode (0x0D) Register

Address	OTP?	Name	Type	Bit values								Initial value							
				B7	B6	B5	B4	B3	B2	B1	B0								
0x0D	No	RDDIM (Read Display Image Mode)	R	0	0	D5	D4	D3	GAMMA				N/A						
				where:															
				D7	Reserved (Vertical Scroll)														
				D6	Reserved (Horizontal Scroll)														
				D5	Inversion Status														
				D4	All Pixels ON														
				D3	All Pixels OFF														

### Description

The Read Display Image Mode returns the current display status as follows.

- Bit D7 – Reserved (Vertical Scrolling)  
This is unused and should return '0'.
- Bit D6 – Reserved (Horizontal Scrolling)  
This is unused and should return '0'.
- Bit D5 – Inversion ON/OFF  
'0' = Inversion OFF.  
'1' = Inversion ON.
- Bit D4 – All Pixels ON, Note 1  
'0' = All Pixels ON is not active.  
'1' = All Pixels ON.
- Bit D3 – All Pixels OFF, Note 1  
'0' = All Pixels OFF is not active.  
'1' = All Pixels OFF.
- Bits D2, D1, D0 – Gamma Curve Selection.  
If no curve has been selected by GAMSET (0x26), then return '111' else return:

D2	D1	D0	Description
0	0	0	GC0: OTP <sub>1</sub>
0	0	1	GC1: OTP <sub>2</sub>
0	1	0	GC2: OTP <sub>3</sub>
0	1	1	GC3: OTP <sub>4</sub>
1	X	X	Not Defined

### Restrictions

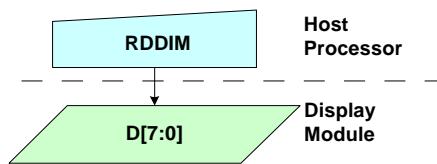
None.

### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power On Sequence	0x00
SW Reset	0x00
HW Reset	0x00

**Flow Chart****9.10 Read Display Signal Mode – RDDSM (0xOE)****Bit Definitions****Table 9-12: Read Display Signal Mode (0xOE) Register**

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0xOE	No	RDDSM (Read Display Signal Mode)	R	D7	D6	D5	D4	D3	D2	0	0	N/A	
				where:									
				D7	Tearing Effect Line ON/OFF								
				D6	Tearing Effect Output Line Mode								
				D5	Horizontal Sync (new slice)								
				D4	Vertical Sync (RSYNC)								
				D3	Pixel Clock								
				D2	Data Enable								

**Description**

The Read Display Signal Mode returns the current display status as follows.

- Bit D7 – Tearing Effect Line ON/OFF  
 ‘0’ = Tearing Effect Line OFF.  
 ‘1’ = Tearing Effect Line ON.
- Bit D6 – Tearing Effect Line Output Mode  
 ‘0’ = Mode 1, V-Blanking only.  
 ‘1’ = Mode 2, both H-Blanking and V-Blanking.
- Bit D5 – Horizontal Sync ON/OFF, Notes 1, 2  
 ‘0’ = Horizontal Sync. bit/line is OFF (“Low”).  
 ‘1’ = Horizontal Sync. bit/line is ON (“High”).
- Bit D4 – Vertical Sync ON/OFF, Notes 1, 3  
 ‘0’ = Vertical Sync. bit/line is OFF (“Low”).  
 ‘1’ = Vertical Sync. bit/line is ON (“High”).
- Bit D3 – Pixel Clock ON/OFF, Notes 1, 2  
 ‘0’ = PCLK line is OFF (“Low”).  
 ‘1’ = PCLK line is ON (“High”).
- Bit D2 – Data Enable On/Off, Notes 1, 2  
 ‘0’ = DE bit/line is OFF (“Low”).  
 ‘1’ = DE bit/line is ON (“High”).

- Bit D1 – Reserved  
This is not used and should return '0'.
- Bit D0 – Reserved  
This is not used and should return '0'.

Note: When bit D0 of DCSCTL (0xC0) is clear and the RGB mode is being used these signals represent the external signals presented to the interface when the command was received. In MPU mode they represent the internally generated equivalent signal.

#### Restrictions

None.

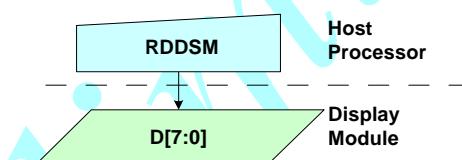
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	0x00
SW Reset	No change
HW Reset	0x00

#### Flow Chart



## 9.11 Read Display Self-Diagnostic Result – RDDSDR (0x0F)

#### Bit Definitions

Table 9-13: Read Display Self-Diagnostic Result (0x0F) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x0F	No	RDDSDR (Read Display Self-Diagnostic Result)	R	D7	D6	D5	D4	0	0	0	0	N/A	
				where:									
				D7	Register Loading Detection								
				D6	Functionality Detection								
				D5	Chip Attachment Detection								
				D4	Display Glass Break Detection								

#### Description

The Read Display Self-Diagnostic Result returns the current display status as follows.

- Bit D7 – Register Loading Detection  
See section
- Bit D6 – Functionality Detection  
See section section 7.6.2
- Bit D5 – Chip Attachment Detection  
Not implemented, returns 0.

- Bit D4 – Display Glass Break Detection  
Not implemented, returns 0.
- Bit D3 – Reserved  
This is unused and should return '0'.
- Bit D2 – Reserved  
This is unused and should return '0'.
- Bit D1 – Reserved  
This is unused and should return '0'.
- Bit D0 – Reserved  
This is unused and should return '0'.

#### Restrictions

None.

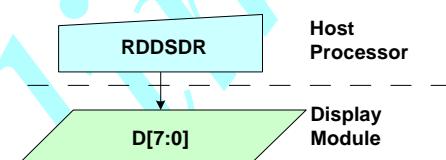
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	0x00
SW Reset	No change
HW Reset	0x00

#### Flow Chart



## 9.12 Sleep In – SLPIN (0x10)

#### Bit Definitions

Table 9-14: Sleep In (0x10) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x10	No	SLPIN (Sleep In)	C	---	---	---	---	---	---	---	---	0x00

#### Description

This command causes the display module to enter the Sleep mode. In this mode, all unnecessary blocks inside the display module are disabled except interface communication. This is the lowest active power mode the display module supports (see description of power modes in section 7.1).

In the Sleep Mode, DBI or DSI Command Modes remain operational and the frame memory maintains its contents. The host processor continues to send PCLK, HS and VS information for two frames after this command is sent when the display module is in Normal mode.

The following conditions will apply:

- Display turns OFF (Anodes connected to VL, Cathodes to VSSDISPLAY).
- Oscillator stops.
- Display internal bias / cascode voltage generator and reverse bias regulators are turned OFF.
- The DC:DC is an external circuit and could be active in this mode.

The interface is fully functional in the Sleep Mode, and Control Register data can be transferred. The RAM is not accessible unless the oscillator is manually started.

#### Restrictions

This command has no effect when the display module is already in Sleep Mode.

The host processor must wait five milliseconds before sending any new commands to a display module following this command to allow time for the supply voltages and clock circuits to stabilize.

The host processor must wait 120 milliseconds after sending a SLOUT (0x11) command before sending a SLPIN (0x10) command.

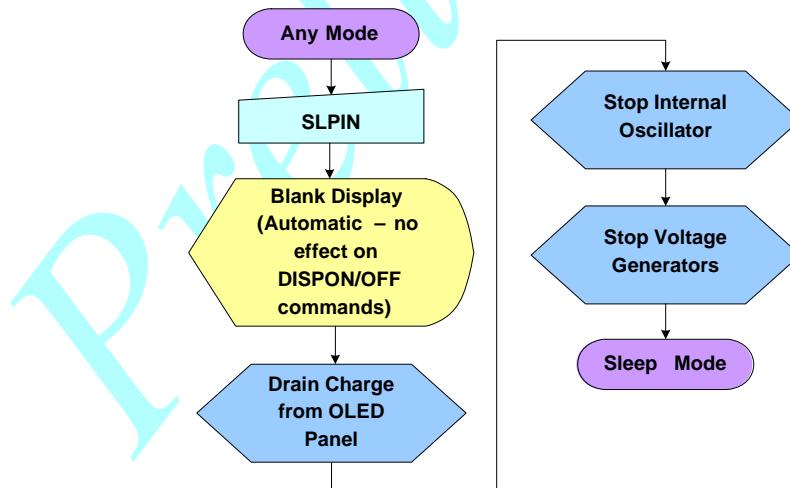
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	Sleep In
SW Reset	Sleep In
HW Reset	Sleep In

#### Flow Chart



## 9.13 Sleep Out – SLPOUT (0x11)

Table 9-15: Sleep Out (0x11) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x11	No	SLPOUT (Sleep In)	C	---								0x00

### Description

This command turns OFF Sleep Mode.

In this mode the internal voltage generators are enabled, the internal oscillator is started, and panel scanning is started. If the DISPON (0x29) is set then the contents of the memory are displayed.

### Restrictions

This command causes no visible effect on the display device if the display module is not in Sleep Mode. The host is likely to periodically send this command as a form of ESD robustness/recovery.

The host processor must wait 70 milliseconds after sending this command before sending another command. This delay allows the supply voltages and clock circuits to stabilize.

The host processor must wait 120 milliseconds after sending a SLPOUT (0x11) command before sending a SLPIN (0x10) command.

The display module loads its default values to the registers when exiting the Sleep Mode. There is no abnormal visual effect on the display device when loading the registers if the factory default and register values are unchanged or when the display module is not in Sleep Mode.

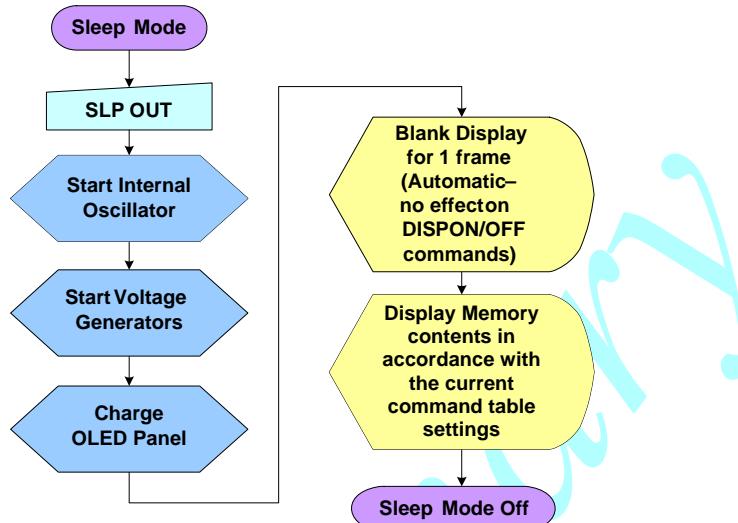
The display module runs the self-diagnostic functions after this command is received. See section 7.6 for a description of the self-diagnostic functions.

### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power On Sequence	Sleep In
SW Reset	Sleep In
HW Reset	Sleep In

**Flow Chart****9.14 Partial Mode On – PTLON (0x12)****Bit Definitions****Table 9-16: Partial Mode On – PTLON Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x12	No	PTLON (Partial Mode On)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command turns on Partial Mode. The Partial Mode window is described by the Partial Area command (0x30). To leave Partial MODE, the Normal Display Mode ON command (0x13) should be written.

**Restrictions**

This command has no effect when Partial Mode is active.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	Normal Display Mode ON
SW Reset	Normal Display Mode ON
HW Reset	Normal Display Mode ON

**Flow Chart**

See Partial Area command (0x30).

## 9.14.1

### 9.15 Normal Mode ON – NORON (0x13)

#### Bit Definitions

Table 9-17: Normal Mode ON (0x13) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x13	No	NORON (Normal Mode On)	C	---	---	---	---	---	---	---	---	0x00

#### Description

This command returns the display to Normal Mode. Normal Mode is defined as Partial Display mode OFF.

#### Restrictions

This command has no effect when Normal Display Mode is already active.

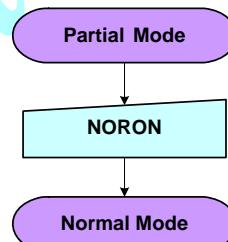
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power On Sequence	Normal Display Mode On
SW Reset	Normal Display Mode On
HW Reset	Normal Display Mode On

#### Flow Chart



### 9.16 Inversion Mode OFF – INVMOFF (0x20)

#### Bit Definitions

Table 9-18: Inversion Mode OFF (0x20) Register

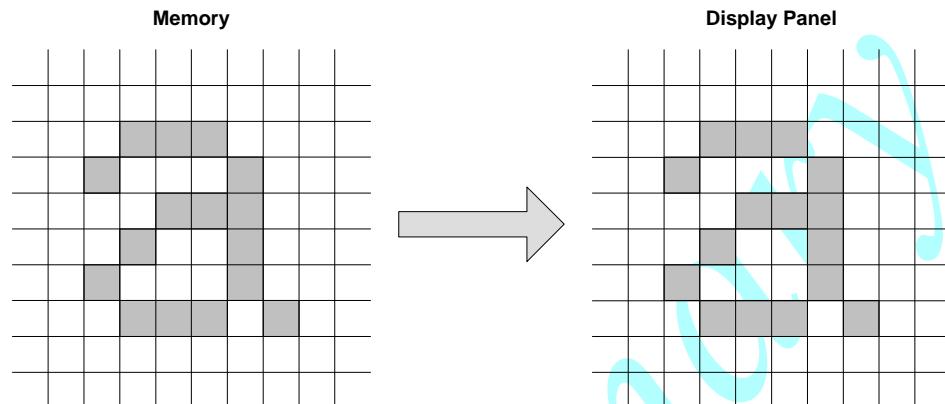
Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x20	No	INVMOFF (Inversion Mode Off)	C	---	---	---	---	---	---	---	---	0x00

#### Description

This command causes the display module to stop inverting the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.

The inversion mode off is achieved in the SmartXtend™ Engine by copying the pixels during the DTRAN (as this will affect the calculated scale factor) and FLOW phases. Writing this command only takes effect during the DTRAN of the next refresh period.

**Figure 9-2: Exit Inversion Mode**



#### Restrictions

This command has no effect when the display module is not inverting the display image.

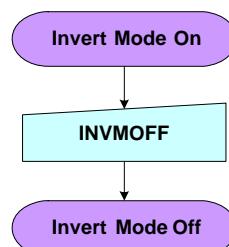
#### Register Availability

Mode	Availability
• Sleep	Yes
• Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	Inversion OFF
SW Reset	Inversion OFF
HW Reset	Inversion OFF

#### Flow Chart



## 9.17 Inversion Mode ON – INVMON (0x21)

### Bit Definitions

Table 9-19: Inversion Mode ON (0x21) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x21	No	INVMON (Inversion Mode On)	C	---	---	---	---	---	---	---	---	0x00

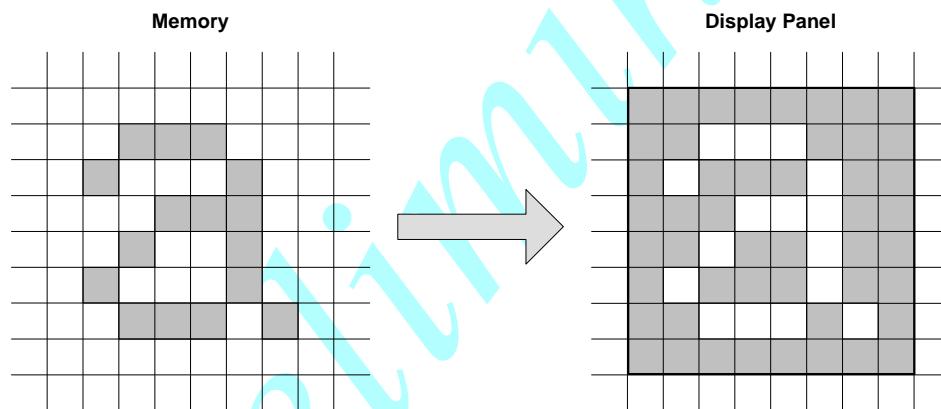
### Description

This command causes the display module to invert the image data on the display device. The frame memory contents remain unchanged. No status bits are changed.

The inversion mode is achieved in the SmartXtend™ Engine by inverting the pixels during the DTRAN (as this will affect the calculated scale factor) and FLOW phases. Writing this command only takes effect during the DTRAN of the next refresh period.

### Restrictions

Figure 9-3: Enter Inversion Mode



This command has no effect when the display module is already inverting the display image.

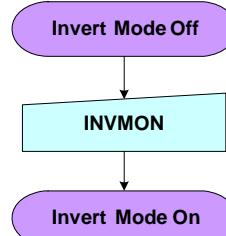
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Inversion OFF
SW Reset	Inversion OFF
HW Reset	Inversion OFF

### Flow Chart



## 9.18 All Pixels OFF – ALLPIXOFF (0x22)

### Bit Definitions

Table 9-20: All Pixels OFF (0x22) Register

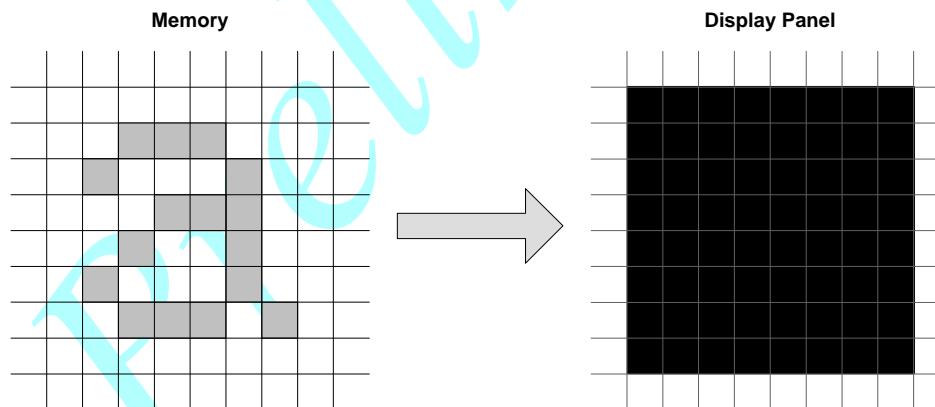
Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x22	No	ALLPIXOFF (All Pixels OFF)	C	---	---	---	---	---	---	---	---	0x00

### Description

This command causes the display module to turn all pixels OFF, displaying a black image. The frame memory contents remain unchanged. No status bits are changed.

To leave All Pixels OFF mode, the host must write one of the display related commands – NORON (0x13), PTION (0x12), ALLPIXON (0x23), INVON (0x21), INVOFF(0x20) or clear the PIXEL field in the ALGDISP (0xC9) register.

Figure 9-4: Enter All Pixels OFF Mode



### Restrictions

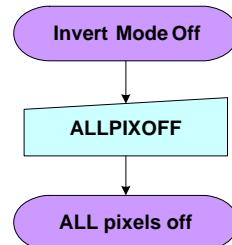
This command has no effect when the display module is already driving all pixels OFF.

### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power On Sequence	Normal Mode
SW Reset	Normal Mode
HW Reset	Normal Mode

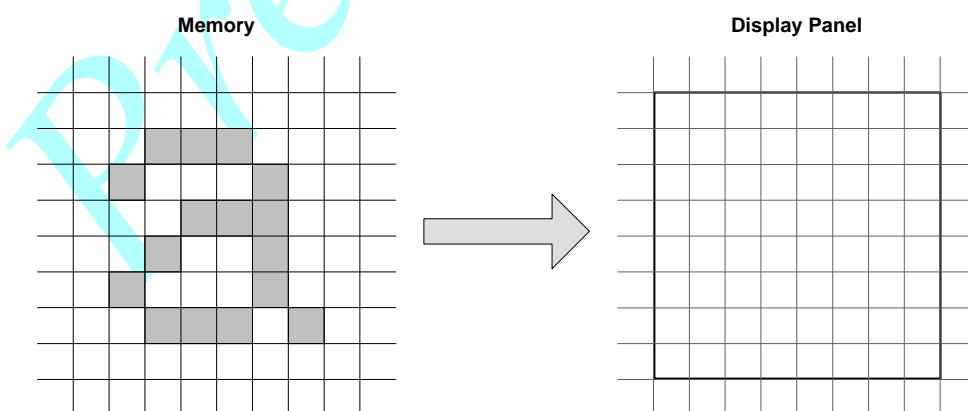
**Flow Chart****9.19 All Pixels On – ALLPIXON (0x23)****Bit Definitions****Table 9-21: All Pixels On (0x23) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x23	No	ALLPIXON (All Pixels On)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command causes the display module to turn all pixels off, displaying a black image. The frame memory contents remain unchanged. No status bits are changed.

To leave All Pixels On mode, the host must write one of the display related commands – NORON (13<sub>H</sub>), PTLON (12<sub>H</sub>), ALLPIXOFF (22<sub>H</sub>), INVON (21<sub>H</sub>), or INVOFF(20<sub>H</sub>). Or clear the PIXEL field in the ALGDISP (49<sub>H</sub>) register.

**Figure 9-5: Enter All Pixels ON Mode****Restrictions**

This command has no effect when the display module is already driving all pixels on.

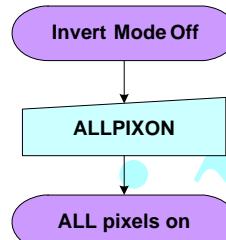
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Normal Mode
SW Reset	Normal Mode
HW Reset	Normal Mode

### Flow Chart



## 9.20 Set Gamma Curve – GAMSET (0x26)

### Bit Definitions

Table 9-22: Set Gamma Curve (0x26) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x26	Yes	GAMSET (Set Gamma Curve)	W		GC[7:0]							0x01
					GC[7:0]:							
				0x00	No Gamma Curve Selected							
				0x01	GC0: y = OTP <sub>1</sub>							
				0x02	GC1: y = OTP <sub>2</sub>							
				0x04	GC2: y = OTP <sub>3</sub>							
				0x08	GC3: y = OTP <sub>4</sub>							

### Description

This command selects the desired gamma curve for the display device. Four fixed gamma curves are defined in section 6.3. A curve is selected by setting the appropriate bit in the parameter as described in the following table.

When no gamma curve is selected the gamma table is bypassed.

### Restrictions

Values of GC[7:0] not shown in table above are invalid and the currently-active Gamma curve will not change until a valid value is received.

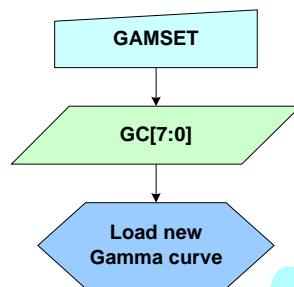
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power ON Sequence	0x01
SW Reset	0x01
HW Reset	0x01

Flow Chart



## 9.21 Display OFF – DISPOFF (0x28)

Bit Definitions

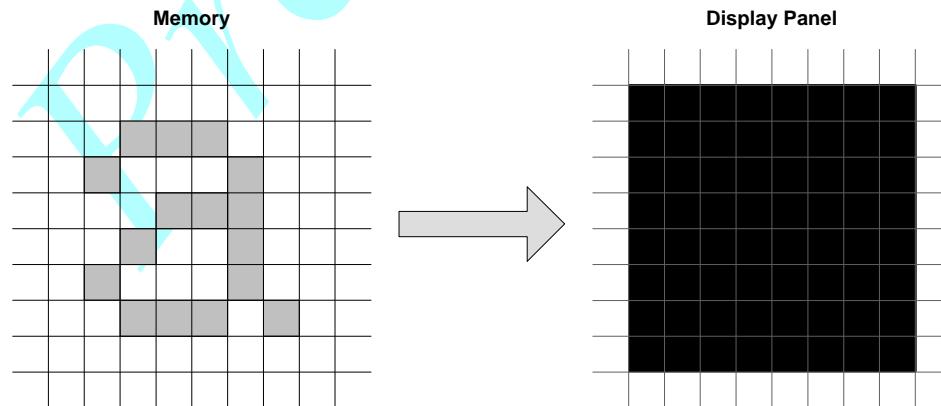
Table 9-23: Display OFF (0x28) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x28	No	DISPOFF (Display Off)	C	---	---	---	---	---	---	---	---	0x00

### Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

Figure 9-6: Enter Display OFF



### Restrictions

This command has no effect when the module is already in Display OFF mode.

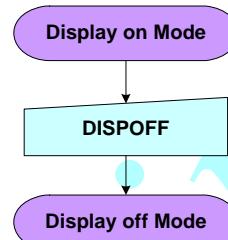
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

### Flow Chart



## 9.22 Display ON – DISPON (0x29)

### Bit Definitions

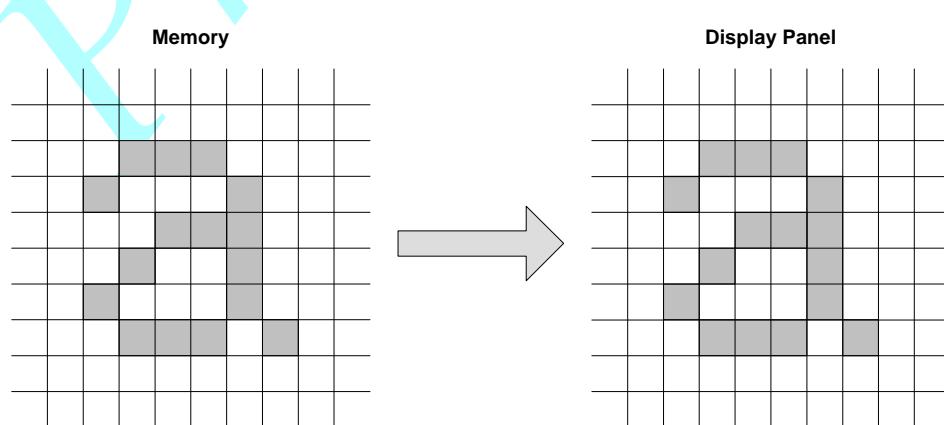
Table 9-24: Display OFF (0x28) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x29	No	DISPON (Display ON)	C	---	---	---	---	---	---	---	---	0x00

### Description

This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.

Figure 9-7: Enter Display OFF



### Restrictions

This command has no effect when the module is already in Display ON mode.

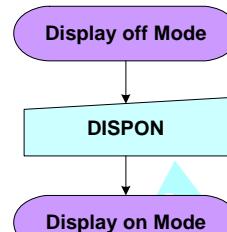
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

#### Flow Chart



## 9.23 Column Address Set – CASET (0x2A)

#### Bit Definitions

Table 9-25: Column Address Set (0x2A) Register

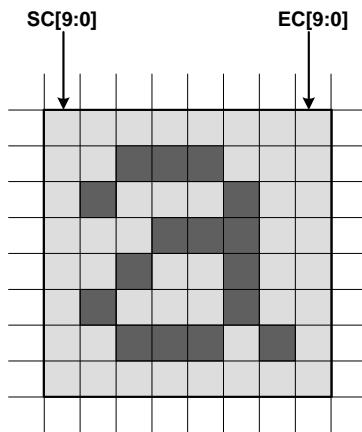
Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x2A	Yes	CASET (Column Address Set)	W	0	0	0	0	0	0	SC[9:8]		0x00
				SC[7:0]								0x00
				0	0	0	0	0	0	EC[9:8]		0x00
				EC[7:0]								0xEF

#### Description

This command is used to define an area of frame memory which the MPU can access. It has no effect on any other driver status.

The values of SC[9:0] and EC[9:0] are referred when a RAMWR command is received. Each value represents one column line in the Frame Memory.

**Figure 9-8: Column Address Set**



## Restrictions

SC[9:0] always must be equal to or less than EC[9:0]. When SC[9:0] or EC[9:0] is greater than 0x00EF (when MADCTL's B5 = 0) or 0x013F (When B5 = 1 in the MADCTL (0x36) register), data out of range will be ignored.

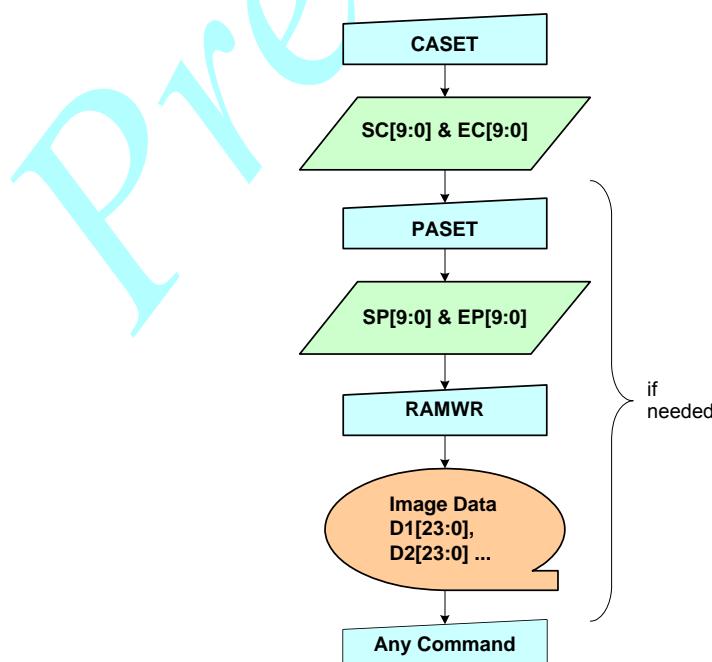
## Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

## Default

Status	Default Value	
Power ON Sequence	SC[9:0] = 0x0000	EC[9:0] = 0x00EF
SW Reset	SC[9:0] = 0x0000	If MADCTL B5 = 0: EC[9:0] = 0x00EF If MADCTL B5 = 1: EC[9:0] = 0x013F
HW Reset	SC[9:0] = 0x0000	EC[9:0] = 0x00EF

## Flow Chart



## 9.24 Page Address Set – PASET (0x2B)

### Bit Definitions

Table 9-26: Page Address Set (0x2B) Register

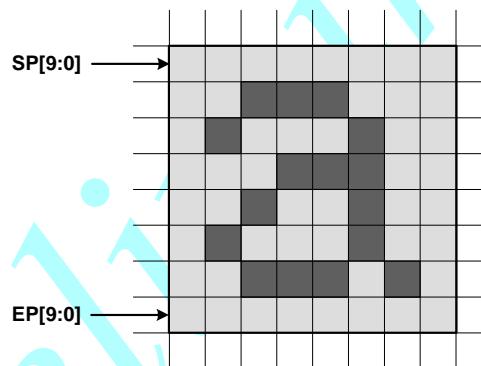
Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x2B	Yes	PASET (Page Address Set)	W	0	0	0	0	0	0	SP[9:8]		0x00
				SP[7:0]								0x00
				0	0	0	0	0	0	EP[9:8]		0x01
				EP[7:0]								0x3F

### Description

This command is used to define an area of frame memory which the MPU can access. It has no effect on any other driver status.

The values of SP[9:0] and EP[9:0] are referred when a RAMWR command is received. Each value represents one page line in the Frame Memory.

Figure 9-9: Page Address Set



### Restrictions

SP[9:0] always must be equal to or less than EP[9:0]. When SP[9:0] or EP[9:0] is greater than 0x013F (When MADCTL's B5 = 0) or 0x00EF (When B5 = 1 in the MADCTL (0x36) register), data out of range will be ignored.

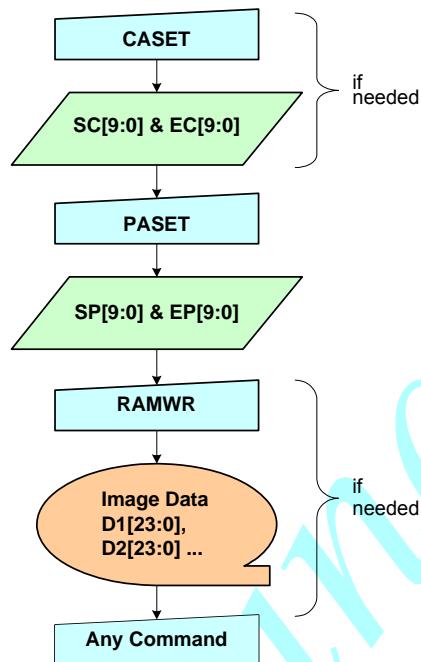
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value	
Power ON Sequence	SP[9:0] = 0x0000	EP[9:0] = 0x013F
SW Reset	SP[9:0] = 0x0000	If MADCTL's B5 = 0: EP[9:0] = 0x013F If MADCTL's B5 = 1: EP[9:0] = 0x00EF
HW Reset	SSP[9:0] = 0x0000	EP[9:0] = 0x013F

### Flow Chart



## 9.25 Write Memory Start – RAMWR (0x2C)

### Bit Definitions

**Table 9-27: Write Memory Start (0x2C) Register**

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x2C	No	RAMWR (Write Memory Start)	W	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									

### Description

This command is used to transfer data from MPU to frame memory. It has no effect on any other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different, depending on the MADCTL setting. Sending any other command (apart from RAMWRC) will stop the Frame Write process.

If B5 = 0 in the MADCTL (0x36) register:

The column and page registers are reset to the Start Column (SC) and Start Page (SP) values, respectively.

Pixel Data 1 is stored in frame memory at (SC, SP). The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.

If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are ignored.

If MADCTL B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively.

Pixel Data 1 is stored in frame memory at (SC, SP). The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are ignored.

### Restrictions

In Sleep Mode the oscillator must be started before the RAM can be accessed.

A RAMWR (Memory Write) command should follow a CASET, PASET or MADCTL command to define the write location. Otherwise, data written with RAMWR and any following RAMWRC commands will be written to undefined locations.

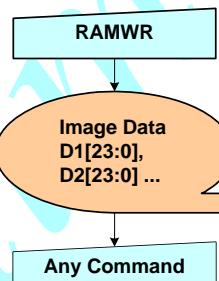
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Contents of memory is set to zero by BIST Engine command
SW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CS is set
HW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CH is set

### Flow Chart



## 9.26 Read Memory Start – RAMRD (0x2E)

### Bit Definitions

Table 9-28: Read Memory Start (0x2E) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x2E	No	RAMRD (Read Memory Start)	R	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									

### Description

This command is used to transfer data from the frame memory to the MPU. It has no effect on any other driver status.

When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different, depending on the MADCTL setting. Sending any other command (apart from RAMWRC) will stop the Frame Read process.

If B5 = 0 in the MADCTL (0x36) register:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively.

Pixel Data 1 is read back from frame memory at (SC, SP). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read back from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are returned as zero.

If B5 = 1:

The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively.

Pixel Data 1 is read back from frame memory at (SC, SP). The page register is then incremented and pixels are read back from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read back from the frame memory until the column register equals the End column (EC) value and the page register equals 1524 the EP value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are returned as zero.

### Restrictions

In Sleep Mode the oscillator must be started before the RAM can be accessed. This command is not available in Test Mode and will return zero.

Regardless of the color mode set in COLMOD (0x3A), the pixel format returned by RAMRD is always 24-bit so there is no restriction on the length of data. The dummy read is only a single transfer (it does not represent the size of a pixel).

It takes a reasonable amount of time to retrieve the data from the RAM and so the MPU must wait 10  $\mu$ s between parameter / sequential data reads. A full image download will take about 1 second ( $10e-6 \times 320 \times 240$ ).

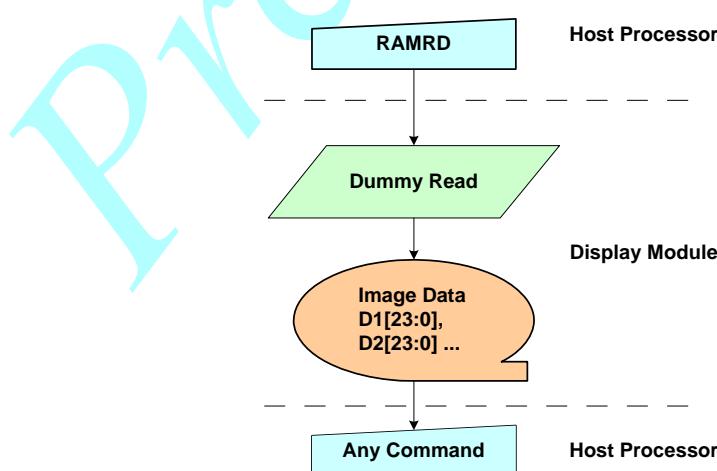
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Contents of memory is set to zero by BIST Engine command
SW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CS is set
HW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CH is set

### Flow Chart



## 9.27 Partial Area – PTLAR (0x30)

### Bit Definitions

Table 9-29: Partial Area (0x30) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x30	No	PTLAR (Partial Area)	W	0	0	0	0	0	0	SR[9:8]		0x00
				SR[7:0]								0x00
				0	0	0	0	0	0	ER[9:8]		0x01
				ER[7:0]								0x3F

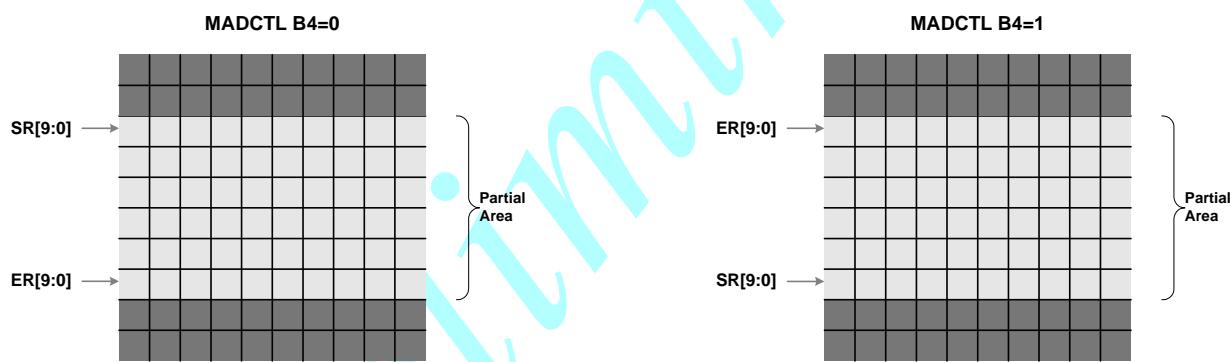
### Description

This command defines the Partial Mode display area. There are 2 parameters associated with this command: the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in Figure 9-10 and Figure 9-11 below.

SR and ER refer to the Frame Memory Line Pointer.

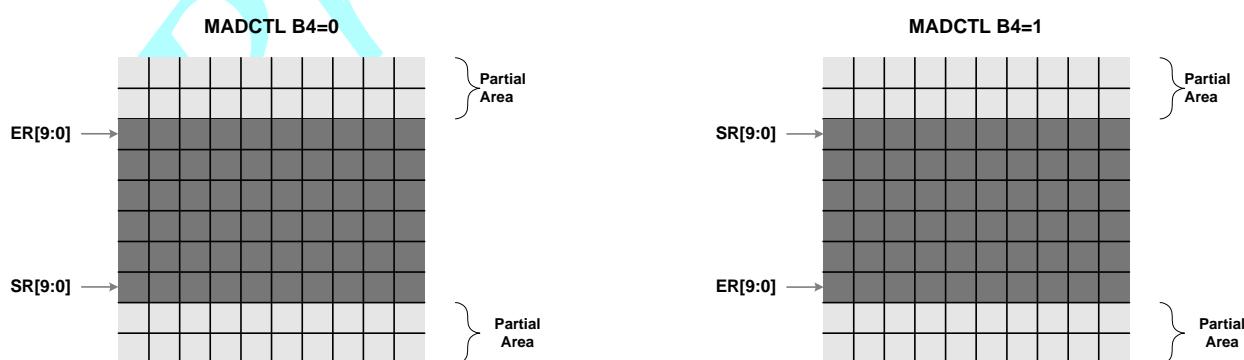
If Start Row < End Row:

Figure 9-10: Partial Area with Start Row < End Row



If End Row < Start Row:

Figure 9-11: Partial Area with End Row < Start Row



If End Row = Start Row then the Partial Area will be one row deep.

### Restrictions

SR[9:0] and ER[9:0] cannot both be 0x0000 nor can either exceed 0x013F.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value	
Power ON Sequence	SR[9:0] = 0x0000	ER[9:0] = 0x013F
SW Reset	SR[9:0] = 0x0000	ER[9:0] = 0x013F
HW Reset	SR[9:0] = 0x0000	ER[9:0] = 0x013F

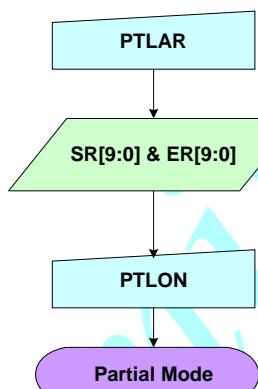
**Flow Chart****9.28 Tearing Effect Off – TEOFF (0x34)****Bit Definitions**

Table 9-30: Tearing Effect Off (0x34) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x34	No	TEOFF (Tearing Effect Line Off)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.

**Restrictions**

This command has no effect when Tearing Effect output is already off.

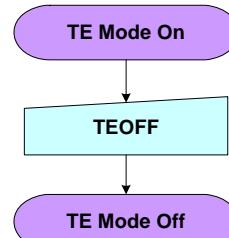
**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	OFF
SW Reset	OFF
HW Reset	OFF

### Flow Chart



## 9.29 Tearing Effect Off – TEON (0x35)

### Bit Definitions

**Table 9-31: Tearing Effect Off (0x34) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x35	No	TEON (Tearing Effect Line ON)	C	---	---	---	---	---	---	---	---	0x00

### Description

This command is used to turn on (Active Low) the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line ON has one parameter which describes the mode of the Tearing Effect Output Line.

During Sleep In Mode with Tearing Effect Line ON, Tearing Effect Output pin will be active Low.

The TE pin is also affected by the TESLSET (0x44) and DCSCTL (0xC0) commands - see section 6.2.2.1.

**Figure 9-12: Tearing Effect Modes**

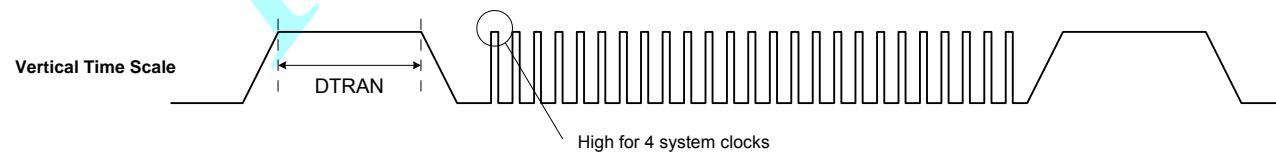
When M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When M=1:

The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:



### Restrictions

This command has no effect when the Tearing Effect output is already off.

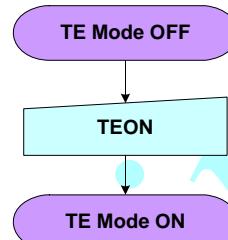
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power ON Sequence	OFF
SW Reset	OFF
HW Reset	OFF

### Flow Chart



## 9.30 Memory Access Control – MADCTL (0x36)

### Bit Definitions

Table 9-32: Memory Access Control (0x36) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x36	Yes	MADCTL (Memory Access Control)	W	D7	D6	D5	-	D3	0	0	0		
				where:									
				D7	Page Address Order								
				D6	Column Address Order								
				D5	Page/Column Order								
				D4									
				D3	RGB/BGR Order								

### Description

This command sets the data order for transfers:

1. from the host processor to the frame memory of the display module (bits B[7:5]) and
  2. from the frame memory of the display module to the display device (bits B[4:3]).
- Bits B[7:5] The effect of these bits on the displayed image is shown below in Figure 9-13:

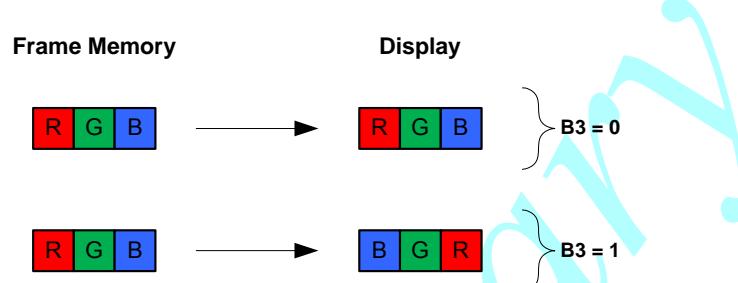
Figure 9-13: Effect of MADCTL Bits B[7:5]

Image in Memory	B7	B6	B5
<b>Normal</b>  SP = 0 EP = 319 SC = 0 EC = 239	0	0	0
<b>V-Flip, Rot 270°</b>  SC = 0 EP = 319 SP = 0 EC = 239	0	0	1
<b>270° Rotation</b>  EC = 319 SC = 0 SP = 0 EP = 239	1	0	1
<b>Horizontal Flip</b>  SP = 0 EP = 319 EC = 239 SC = 0	0	1	0
<b>90° Rotation</b>  SC = 0 EP = 319 EP = 239 SP = 0	0	1	1
<b>180° Rotation</b>  EP = 319 SC = 0 EP = 239 SC = 0	1	1	0
<b>V-Flip, Rot 90°</b>  EC = 319 SC = 0 EP = 239 SP = 0	1	1	1

**Bit B3 - RGB/BGR Order**

This bit controls the RGB data order transferred from the peripheral's frame memory to the display device.

- '0' = Pixels sent in RGB order.
- '1' = Pixels sent in BGR order.

**Figure 9-14: Bit B3 - RGB/BGR Order****Restrictions**

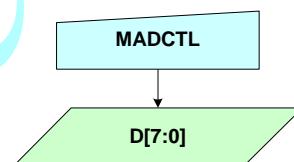
None, but note the special behavior on SW Reset.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	0x00
SW Reset	No Change
HW Reset	0x00

**Flow Chart****9.3.1 Idle Mode Off – IDMOFF (0x38)****Bit Definitions****Table 9-33: Idle Mode OFF (0x38) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x38	No	IDMOFF (Idle Mode Off)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command causes the display module to exit Idle Mode.

**Restrictions**

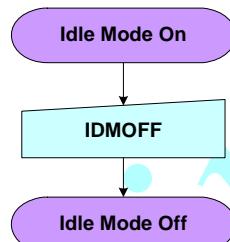
This command has no effect when the display module is not in Idle Mode.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power ON Sequence	Idle OFF
SW Reset	Idle OFF
HW Reset	Idle OFF

**Flow Chart****9.32 Idle Mode On – IDMON (0x39)****Bit Definitions****Table 9-34: Idle Mode OFF (0x38) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x39	No	IDMON (Idle Mode ON)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command is used to enter into Idle Mode. In the idle ON mode, color expression is reduced. The primary and the secondary colors using the MSB's of each R, G and B in the Frame Memory, 8-color depth data is displayed.

**Restrictions**

This command has no effect when the display module is already in Idle Mode.

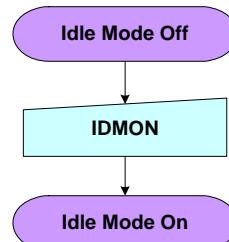
**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power ON Sequence	Idle OFF
SW Reset	Idle OFF
HW Reset	Idle OFF

### Flow Chart



## 9.33 Set Display Pixel Format – COLMOD (0x3A)

### Bit Definitions

**Table 9-35: Set Display Pixel Format (0x3A) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x3A	Yes	COLMOD (Set Display Pixel Format)	W	0	RGBPF			0	MPUPF			0x67

### Description

This command sets the pixel format for the RGB image data used by the interface. The physical mapping of the pixels is given in section 6.2.3. For mappings that have two possible options, the selection is controlled by the DCSCTL (0xC0) command bits D[1:0].

- Bits D[6:4] – RGB Pixel Format Definition
- Bits D[2:0] – MPU Pixel Format Definition
- Bits D7 and D3 are not used.

D6/D2	D5/D1	D4/D0	Description
0	0	0	Reserved
0	0	1	Reserved
0	1	0	8 bits/pixel
0	1	1	12 bits/pixel
1	0	0	Reserved
1	0	1	16 bits/pixel
1	1	0	18 bits/pixel
1	1	1	24 bits/pixel

### Restrictions

There is no visible effect until the frame memory is written.

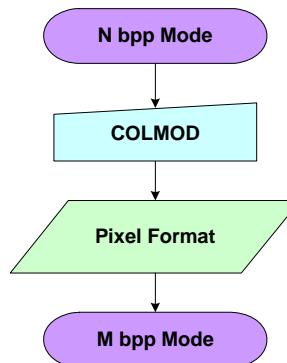
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	0x67
SW Reset	0x67
HW Reset	0x67

### Flow Chart



## 9.34 Memory Write Continue – RAMWRC (0x3C)

### Bit Definitions

Table 9-36: Memory Write Continue (0x3C) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x3C	No	RAMWRC (Memory Write Continue)	W	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									

### Description

This command transfers image data from the host processor to the frame memory of the display module, continuing from the pixel location following the previous RAMWRC (Memory Write Continue) or RAMWR (Memory Write Start) command.

If B5 = 0 in the MADCTL (0x36) register:

Data is written continuing from the pixel location after the write range of the previous RAMWR or RAMWRC. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are ignored.

If B5 = 1:

Data is written continuing from the pixel location after the write range of the previous RAMWR or RAMWRC. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are ignored.

### Restrictions

In Sleep Mode the oscillator must be started before the RAM can be accessed.

A RAMWR (Memory Write Start) command should follow a CASET, PASET or MADCTL command to define the write location. Otherwise, data written with RAMWR and any following RAMWRC commands will be written to undefined locations.

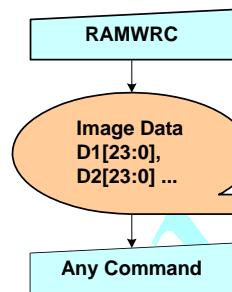
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Contents of memory is set to zero by BIST Engine command
SW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CS is set
HW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CH is set

### Flow Chart



## 9.35 Memory Read Continue – RAMRDC (0x3E)

### Bit Definitions

Table 9-37: Memory Read Continue (0x3E) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0x3E	No	RAMRDC (Memory Read Continue)	R	1 <sup>st</sup> Parameter									
				2 <sup>nd</sup> Parameter									
				...									
				Last Parameter									

### Description

This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous RAMRDC (Memory Read Continue) or RAMRD (Memory Read Start) command.

#### If B5 = 0 in the MADCTL (0x36) register:

Pixels are read continuing from the pixel location after the read range of the previous RAMRD (Memory Rest Start) or RAMRDC (Memory Read Continue). The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read back from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds  $(EC - SC + 1) * (EP - SP + 1)$  the extra pixels are returned as zero.

#### If B5 = 1:

Pixels are read continuing from the pixel location after the read range of the previous RAMRD (Memory Read Start) or RAMRDC (Memory Read Continue). The page register is then incremented and pixels are read back from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read back from the frame memory until the column register equals the End column

(EC) value and the page register equals 1524 the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) \* (EP – SP + 1) the extra pixels are returned as zero.

### Restrictions

In Sleep Mode the oscillator must be started before the RAM can be accessed.

Regardless of the color mode set by COLMOD (0x3A), the pixel format returned by RAMRDC is always 24-bit, so there is no restriction on the length of data.

It takes a reasonable amount of time to retrieve the data from the RAM and so the MPU must wait 10  $\mu$ s between parameter / sequential data reads. A full image download will take about 1 second ( $10e-6 \times 320 \times 240$ ).

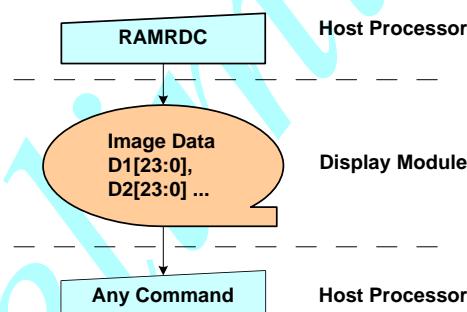
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	Contents of memory set to zero by BIST Engine command
SW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CS is set
HW Reset	Not cleared – Cleared if DCSCTL (0xC0) Bit CH is set

### Flow Chart



## 9.36 Tear Scan Line Set – TESLSET (0x44)

### Bit Definitions

Table 9-38: Tear Scan Line Set (0x44) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x44	Yes	TESLSET (Tear Scan line Set)	W	0	0	0	0	0	0	N[9:8]	N[7:0]	

### Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing bit D4 in MADCTL (Register 0x36).

The Tearing Effect Output line consists of V-Blanking information only such that setting TESLSET with N = 0 is equivalent to TEON with M = 0. The Tearing Effect Output line is active low when the display module is in Sleep Mode.

**Figure 9-15: Tearing Effect scan line modes**

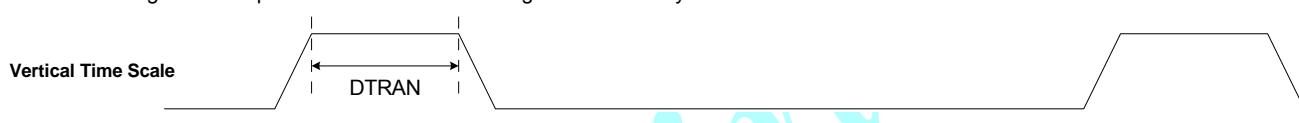
When N=0 it is identical to TEON with M=0:

The Tearing Effect Output line consists of V-Blanking information only:



When N≠0 it uses DTRAN, offset by relevant HLINEs:

The Tearing Effect Output line consists of V-Blanking information only:



### Restrictions

This command takes effect on the frame following the current frame. Therefore, if the Tear Effect (TE) output is already ON, the **TE** output shall continue to operate as programmed by the previous TEON (0x35), or TESLSET, command until the end of the frame.

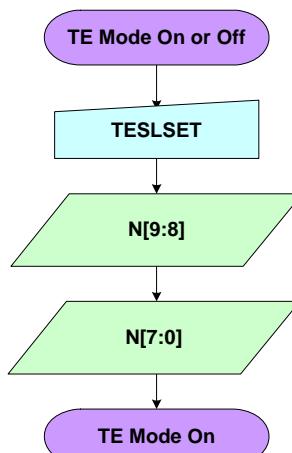
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

### Flow Chart



### 9.37 Current Scan Line – CURSL (0x45)

#### Bit Definitions

Table 9-39: Current Scan Line (0x45) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0x45	No	CURSL (Current Scan line)	R	0	0	0	0	0	0	N[9:8]	N[7:0]	

#### Description

The display module returns the current scan line, N, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V Sync and is denoted as Line 0.

In MPU mode the internal HLINE count is used as an internal scan line count and returned.

When in Sleep Mode, the value returned by CURSL is undefined.

#### Restrictions

None.

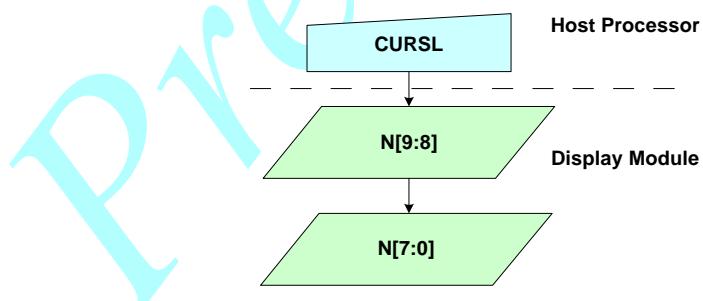
#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

Default

Status	Default Value
Power On Sequence	OFF
SW Reset	OFF
HW Reset	OFF

#### Flow Chart



## 9.38 Read DDB Start – RDDDB (0xA1)

### Bit Definitions

Table 9-40: Read DDB Start (0xA1) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xA1	Yes	RDDDB (Read DDB Start)	R	MSB Supplier ID								0xFF
				LSB Supplier ID								0xFF
				...								...
				Last Parameter								0xFF

### Description

This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that is 8-bytes long.

The data is stored in the OTP from address 0x08 to 0x0F. After all 8-bytes have been read from the OTP the command returns the exit code 0xFF. If the OTP is not programmed then the command simply returns 0xFF.

The format of returned data is as follows:

1. Parameter 1: MS (most significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.
2. Parameter 2: LS (least significant) byte of Supplier ID.
3. Parameter 3: MS (most significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.
4. Parameter 4: LS (least significant) byte of Supplier Elective Data
5. Parameter 5: single-byte Escape or Exit Code (EEC). The code is interpreted as follows:

0xFF - Exit code – there is no more data in the Descriptor Block

0x00 - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI Alliance standard)

Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in MIPI Alliance Standard for Device Descriptor Block (DDB).

### Restrictions

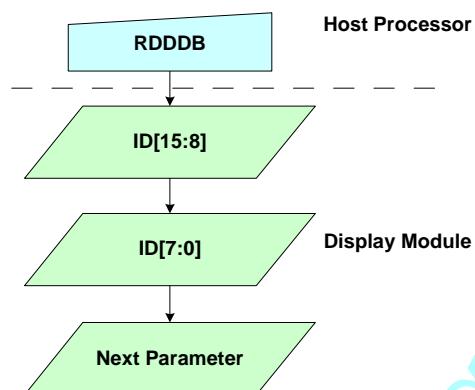
If the OTP is not programmed then the command returns 0xFF.

### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	OFF
SW Reset	OFF
HW Reset	OFF

**Flow Chart****9.39 Oscillator ON – OSCON (0xB2)****Bit Definitions****Table 9-41: Oscillator ON (0xB2) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xB2	No	OSCON (Oscillator ON)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command turns on the oscillator and activates the partial clock tree necessary to write data into the Memory.

**Restrictions**

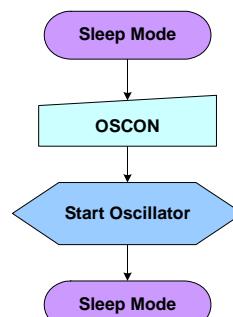
This command has no effect when the oscillator is already running.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	Oscillator OFF
SW Reset	Oscillator OFF
HW Reset	Oscillator OFF

**Flow Chart**

## 9.40 Oscillator OFF – OSCOFF (0xB3)

### Bit Definitions

Table 9-42: Oscillator OFF (0xB3) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xB3	No	OSCOFF (Oscillator OFF)	C	---	---	---	---	---	---	---	---	0x00

### Description

This command turns OFF the oscillator.

### Restrictions

This command has no effect when the oscillator is already stopped. This command is not available in normal Sleep-out Mode (turning OFF the oscillator would be a very bad thing) but is available in Test Mode for current measuring purposes.

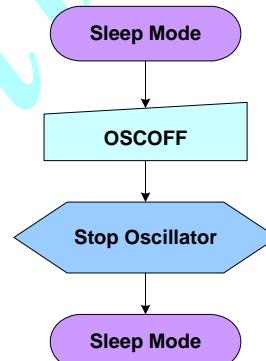
### Register Availability

Mode	Availability
Sleep	Yes
Normal	No

### Default

Status	Default Value
Power ON Sequence	Oscillator OFF
SW Reset	Oscillator OFF
HW Reset	Oscillator OFF

### Flow Chart



## 9.41 Power OFF – PWROFF (0xB4)

### Bit Definitions

Table 9-43: Power OFF (0xB4) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xB4	No	PWROFF (Power OFF)	C	---	---	---	---	---	---	---	---	0x00

**Description**

This command causes the display module to enter the Power OFF mode. In this mode, all blocks inside the display module are disabled, including the interface communication, the internal bias, bandgap and 1.5 V (DVDD) supply are all switched off. This is the lowest power mode – see description of power modes in section 7.1.

To exit the Power OFF mode the RSTB pin must be taken low for 5 $\mu$ s. This will enable the bias, bandgap and 1.5v LDO (note: the digital output will be held in reset until the LDO has reached the required voltage, at which point the reset to the digital will be released and the device will be in "Sleep Mode").

**Restrictions**

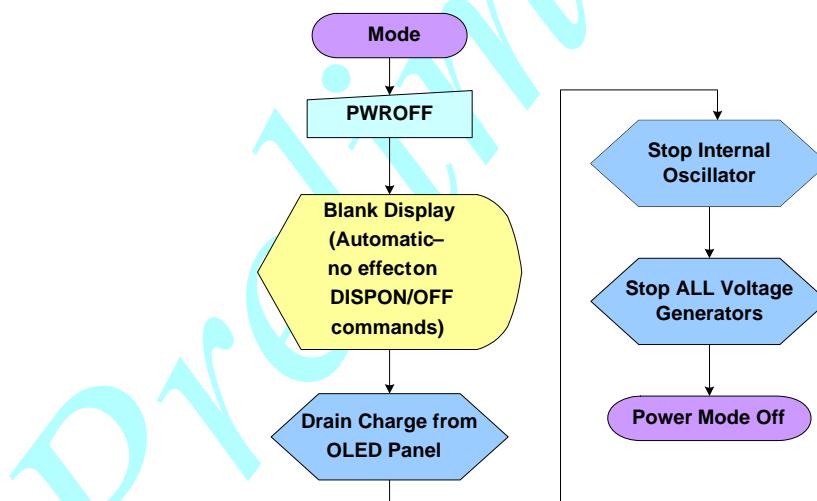
None.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	Sleep IN
SW Reset	Sleep IN
HW Reset	Sleep IN

**Flow Chart**

## 9.42 Dimmer Set – DIMSET (0xB5)

### Bit Definitions

Table 9-44: Dimmer Set (0xB5) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0xB5	No	DIMSET (Dimmer Set)	W	0	0	0	0	0	0	DIM		0x00	
				DIM:									
				00	Normal Mode								
				01	1/2 Bright								
				10	1/4 Bright								
				11	1/8 Bright								

### Description

The DIMSET command sets the current state of the brightness Dimmer. The dimming function is carried out by the algorithm by shifting the data the required number of bits to reduce the luminosity of the picture (this ensures that the peak current can be adjusted to take advantage of the increased scale factor and maintains accurate color balance). The contents of the RAM are not affected, the shift operation happens as the data is read from the shadow RAM. The scale factor is only adjusted on the next DTRAN refresh cycle. The dimmer action is synchronized to a refresh frame.

1. Bits D[7:2] – Reserved  
This is not used and should return '0' when read.
2. Bits D[1:0] – Dimmer Level  
 '00' = Normal action with no shift.  
 '01' = Shift the input data down by one bit.  
 '10' = Shift the input data down by two bits.  
 '11' = Shift the input data down by three bits.

### Restrictions

None.

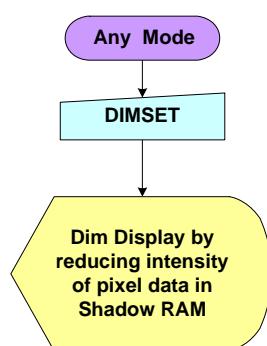
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	0x00
SW Reset	0x00
HW Reset	0x00

### Flow Chart



### 9.43 Brightness Level Monitor – BRIGHTLM (0xB9)

Please refer to Application Note

### 9.44 Brightness Set – BRIGHTSET (0xBA)

Please refer to Brightness Set Application Note

### 9.45 Black/White Convert - BWCONV (0xBB)

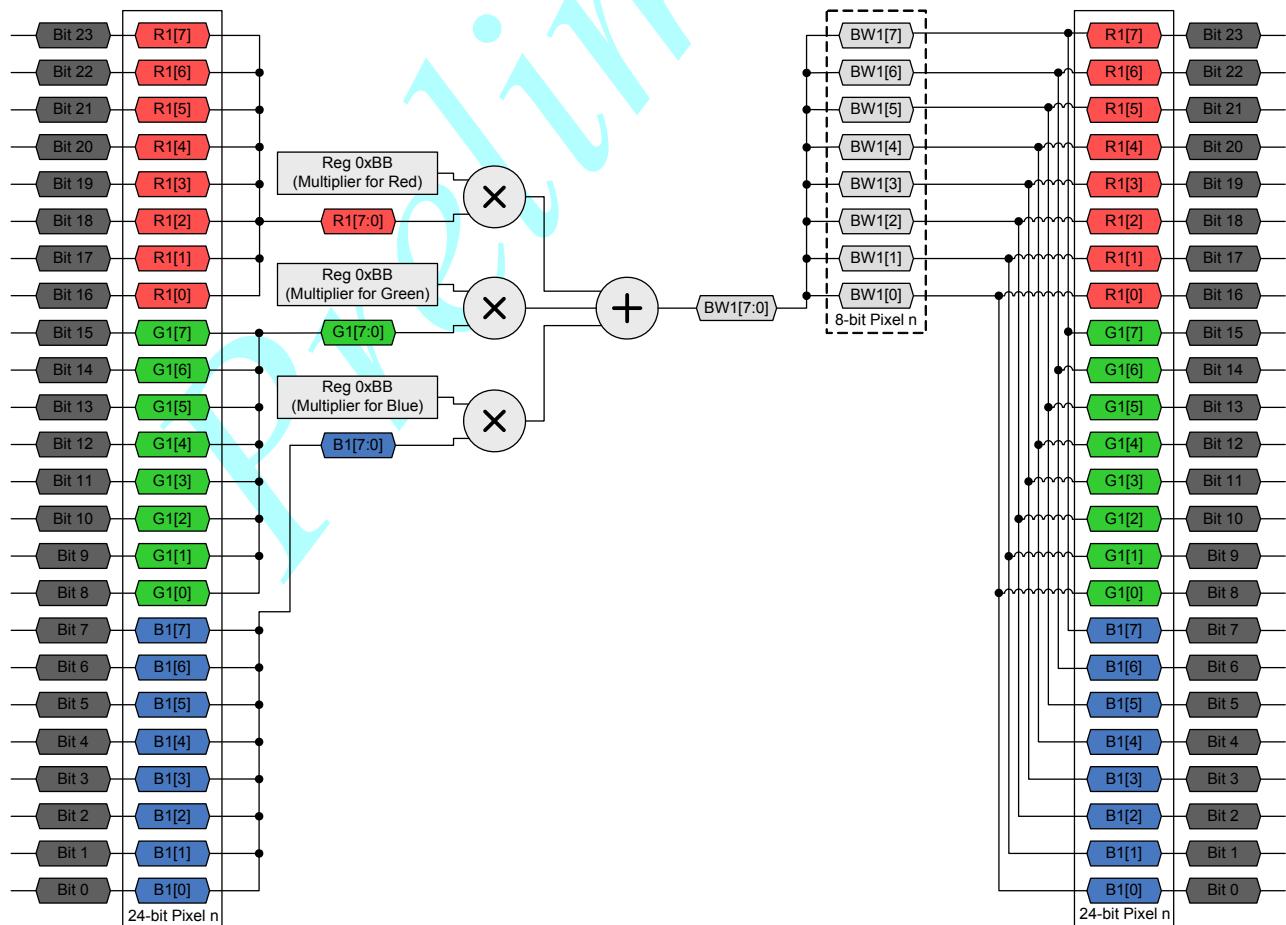
Table 9-45: Manufacturer Base Control Registers

Address	OTP?	Name	R/W?	Bit values								Initial value
				D7	D6	D5	D4	D3	D2	D1	D0	
0xBB	Yes	BWCONV (Black/white convert)	W	Multiplier for Red								0x4D
				Multiplier for Green								0x97
				Multiplier for Blue								0x1C

#### Description

The BWCONV command is used to set the Red, Blue, and Green multipliers for the RGB to B/W channel mixer logic. The sum of the three multipliers must be 0x100. The default values preserve luminosity during the conversion process (see section 6.2.1 on page 46 for details). Conversion happens after the pixel has been expanded to the internal 24-bit format, but before the gamma correction has been applied.

Figure 9-16: 24-bits/pixel, RGB to Grayscale Convert



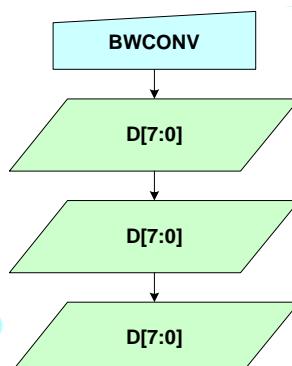
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes
Test	Yes
Scan	No

### Default

Status	Default Value
Power ON Sequence	0x4D, 0x97, 0x1C
SW Reset	0x4D, 0x97, 0x1C
HW Reset	0x4D, 0x97, 0x1C

### Flow Chart



## 9.46 DCS Control – DCSCTL (0xC0)

### Bit Definitions

Table 9-46: DCS Control (0xC0) Register

Address	OTP?	Name	Type	Bit values								Initial value	
				B7	B6	B5	B4	B3	B2	B1	B0		
0xC0	Yes	DCSCTL (DCS Control)	W	BW	BM	CS	CH	TE	SG	RGBOPT	MPUOPT	0x00	
				where:									
				BW	Black and White convert								
				BM	Bottom Mount device								
				CS	Clear Memory on SW Reset								
				CH	Clear Memory on HW Reset								
				TE	Output RSYNC on the TE pin								
				SG	A single Gamma Table								
				D1	RGBOPT for Pixel Format								
				D0	MPUOPT for Pixel Format								

### Description

The DCS Control register controls those options related to the MIPI Display Command Set (DCS) that have alternative functionality.

Bit D7 controls conversion of the image to Black & White. Bit D6 inverts the MADCTL bits 7,6 and 3, as seen by the rest of the system so that, to the outside world, a bottom-mounted device appears to behave exactly the same as a top-mounted one. Bits D[5:4] define the action of the memory clear BIST function after a reset. The MIPI DCS standard leaves the memory unchanged following a reset, but as we are clearing the memory on power-up, it makes sense to offer the same ability following a reset. Bit D3 outputs the DTRAN signal on the TE pin, with the width of the pulse marking the DTRAN refresh cycle. Bit D2 controls the gamma table – in order to save OTP space we interpolate the standard MIPI gamma curves (an 8:1 interpolation gives no more than a single bit error). The single gamma curve option allows a finer granularity of interpolation (2:1) should non-standard curves be required. Bits D[1:0] select between the alternative pixel formats for the RGB and MPU interfaces.

When testing, special care must be given to the BM bit, especially with respect to the different address access modes and the partial area registers.

1. Bit D7 - Black & White convert  
 '0' = do not convert display  
 '1' = convert display to Black & White
2. Bit D6 – Bottom Mount (see section 2.2.1)  
 '0' = Device mounted at top of display.  
 '1' = Device mounted at bottom of display.
3. Bit D5 – Clear Memory on SW Reset  
 '0' = SW Reset leaves RAM unchanged.  
 '1' = SW Reset causes the RAM to be cleared.
4. Bit D4 – Clear Memory on HW Reset  
 '0' = HW Reset leaves RAM unchanged.  
 '1' = HW Reset causes the RAM to be cleared.
5. Bit D3 – Output DTRAN on TE Pin  
 '0' = TE pin action defined by TEON, TEOFF, and TESLSET.  
 '1' = TE pin reflects the internal DTRAN signal.
6. Bit D2 – Single Gamma (see section section 6.3)  
 '0' = Implement 4 gamma curves as specified by GAMSET (0x26).  
 '1' = Implement a higher-resolution single gamma table (all curves map to this).
7. Bit D1 – RGB Option (see section 2.2.1)  
 '0' = Select Pixel Format option 1  
 '1' = Select Pixel Format option 2.
8. Bit D0 – MPU Option (see section 2.2.1)  
 '0' = Select Pixel Format option 1  
 '1' = Select Pixel Format option 2.

#### Restrictions

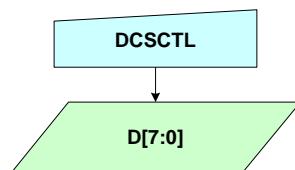
None.

#### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

#### Default

Status	Default Value
Power ON Sequence	0x00
SW Reset	0x00
HW Reset	0x00

**Flow Chart****9.47 RGB Control – RGBCTL (0xC1)****Bit Definitions****Table 9-47: RGB Control (0xC1) Register**

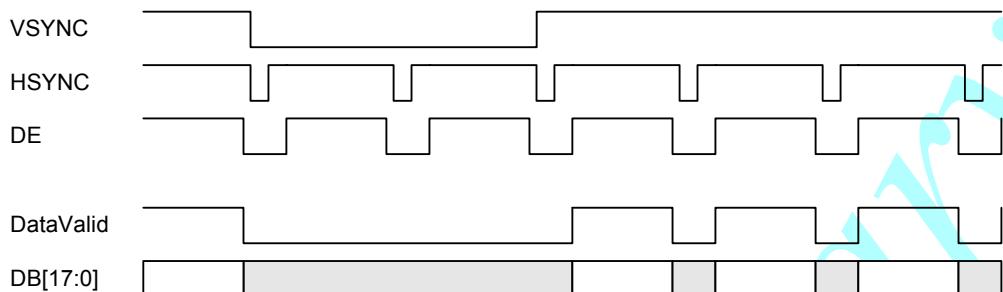
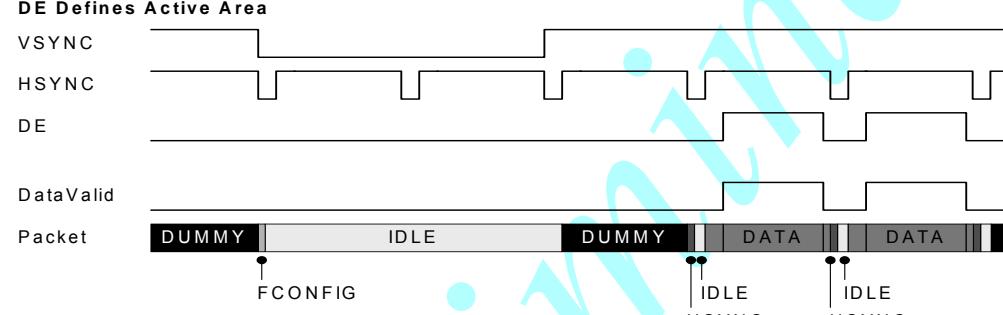
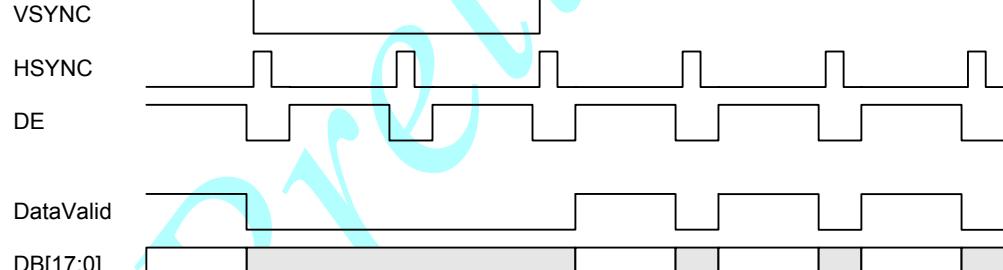
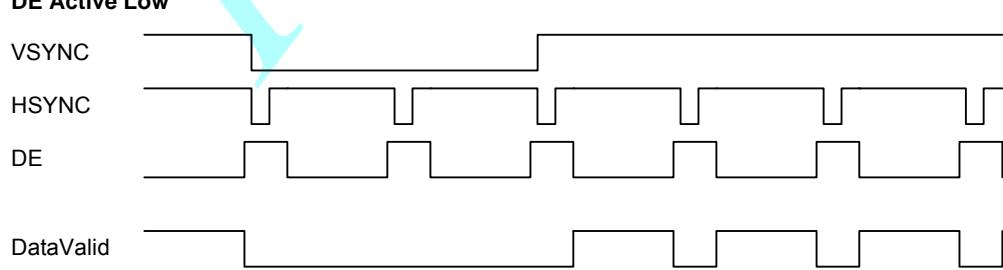
Address	OTP?	Name	Type	Bit values								Initial value			
				B7	B6	B5	B4	B3	B2	B1	B0				
0xC1	Yes	RGBCTL (RGB Control)	W	D7	D6	D5	D4	D3	D2	MODE		0x01			
				where:											
				D7	Syncs latched on falling PCLK										
				D6	DE latched on falling PCLK										
				D5	Data latched on falling PCLK										
				D4	VSYNC active high										
				D3	HSYNC active high										
				D2	DE active low										
				MODE:											
				00	Ignore DE pin										
				01	DE defines Valid Data										
				10	DE defines Active Area										
				11	Reserved										

**Description**

The RGB Control register defines the action of the external RGB mode interface pins, defining the activity levels and on which edge (relative to the external PCLK) a signal is re-timed to before being used internally.

- Bit D7 – SYNCs latched on falling PCLK  
 ‘0’ = HSYNC and VSYNC re-timed to rising edge of PCLK.  
 ‘1’ = HSYNC and VSYNC re-timed to falling edge of PCLK.
- Bit D6 – DE latched on falling PCLK  
 ‘0’ = DE re-timed to rising edge of PCLK  
 ‘1’ = DE re-timed to falling edge of PCLK.
- Bit D5 – DB[17:0] latched on falling PCLK  
 ‘0’ = DB[17:0] re-timed to rising edge of PCLK  
 ‘1’ = DB[17:0] re-timed to falling edge of PCLK.
- Bit D4 – VSYNC active high  
 ‘0’ = VSYNC active low (data is invalid whilst VSYNC is low)  
 ‘1’ = VSYNC active high (data is invalid whilst VSYNC is high).
- Bit D3 – HSYNC active high  
 ‘0’ = HSYNC active low (data is invalid whilst HSYNC is low)  
 ‘1’ = HSYNC active high (data is invalid whilst HSYNC is high).
- Bit D2 – DE active low  
 ‘0’ = DE active high (data is valid/active whilst DE is high)  
 ‘1’ = DE active low (data is valid/active whilst DE is low).

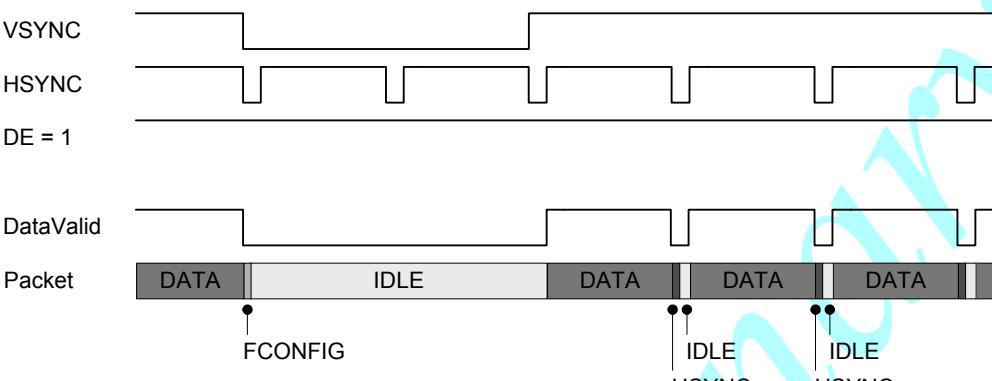
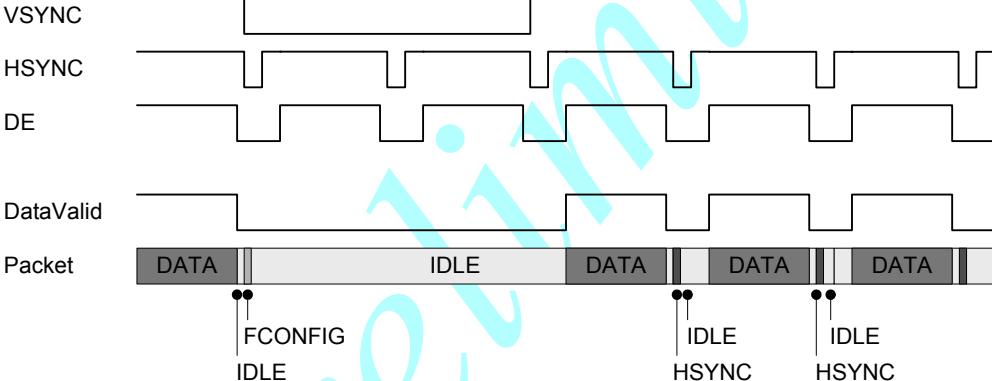
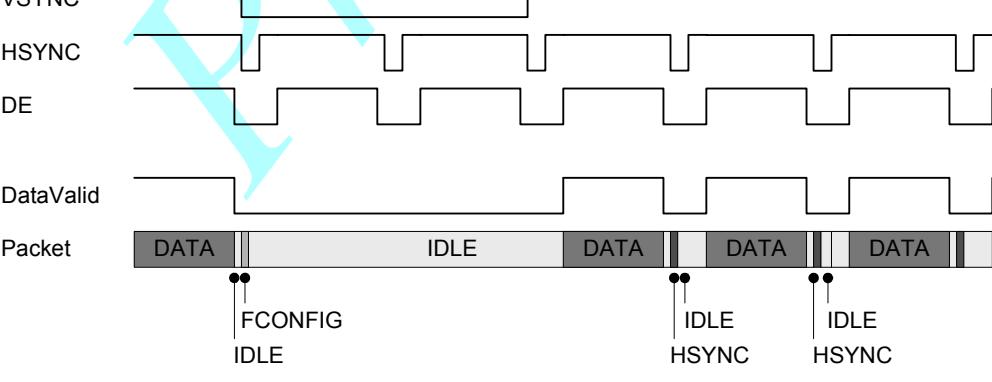
Table 9-48: External RGB Interface Modes

Timing Diagram	RGBCTL Bits B[4:2]
<p><b>Default Settings</b></p> 	0 0 0
<p><b>DE Defines Active Area</b></p> 	1 0 0
<p><b>HSYNC Active High</b></p> 	0 1 0
<p><b>DE Active Low</b></p> 	0 0 1

- Bits D[1:0] - Mode  
 '00' = DE is ignored and assumed always valid.  
 '01' = DE defines valid data.

- '10' = DE defines active area.
- '11' = Reserved.

**Table 9-49: External RGB Interface Modes**

Timing Diagram	RGBCTL Bits B[1:0]
<p><b>DE is Ignored</b></p> 	0 0
<p><b>DE Defines Valid Data</b></p> 	0 1
<p><b>DE Defines Valid Data</b></p> 	1 0

**Restrictions**

None.

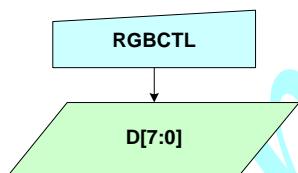
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	0x00
SW Reset	0x00
HW Reset	0x00

### Flow Chart



## 9.48 Serial Interface ID – SERID (0xC2)

### Bit Definitions

Table 9-50: Serial Interface ID (0xC2) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xC2	Yes	SERID (Serial Interface ID)	W	0	0							Slave Address (see Note 1)

Note 1) The slave address is defined in OTP

### Description

The SERID register specifies the slave address that the device will respond to in I<sup>2</sup>C and Dialog 3-wire SPI modes. In SPI mode the 6-bit address is used to specify the top 6-bits of the start code that must be matched before the device will respond to the SPI command. In I<sup>2</sup>C mode, if the Slave Device address matches the transmitted 6-bit address, the DA8620 will send an acknowledgement (ACK) to the host, by pulling **SDA\_SDO** low during the 9<sup>th</sup> **E\_RDB\_SCL** clock pulse. All subsequent transfers will also be acknowledged.

1. Bits D[7:6] – Reserved  
These are not used and should return ‘0’ when read.
2. Bits D[5:0] – Slave Address  
This is the address of the serial slave used in I<sup>2</sup>C or Dialog SPI mode.

### Restrictions

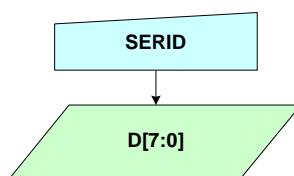
None.

### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	0x00
SW Reset	0x00
HW Reset	0x00

**Flow Chart****9.49 Read Identification 1 – RDID1 (0xDA)****Bit Definitions****Table 9-51: Read Identification 1 (0xDA) Register**

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xDA	Yes	RDID1 (Read Identification 1)	R	Manufacturer ID								0XX

**Description**

This read command returns the 8-bit Display Manufacturer ID. The data returned is the same as that returned by the RDDIDIF (0x04) command.

**Restrictions**

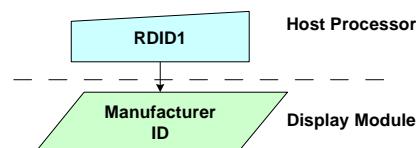
None.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

**Flow Chart**

## 9.50 Read Identification 2 – RDID2 (0xDB)

### Bit Definitions

Table 9-52: Read Identification 2 (0xDB) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xDB	Yes	RDID2 (Read Identification 2)	R	Type and Version								0xYY

### Description

This read command returns the 8-bit display Type and Version. The data returned is the same as that returned by the RDDIDIF (0x04) command.

### Restrictions

None.

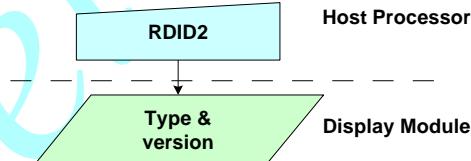
### Register Availability

Mode	Availability
Sleep	Yes
Normal	Yes

### Default

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

### Flow Chart



## 9.51 Read Identification 3 – RDID3 (0xDC)

### Bit Definitions

Table 9-53: Read Identification 3 (0xDC) Register

Address	OTP?	Name	Type	Bit values								Initial value
				B7	B6	B5	B4	B3	B2	B1	B0	
0xDC	Yes	RDID3 (Read Identification 3)	R	Display Module								0xZZ

### Description

This read command returns the 8-bit display Module ID. The data returned is the same as that returned by the RDDIDIF (0x04) command.

### Restrictions

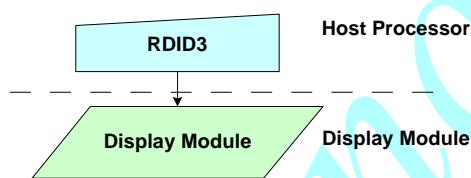
None.

**Register Availability**

Mode	Availability
Sleep	Yes
Normal	Yes

**Default**

Status	Default Value
Power ON Sequence	N/A
SW Reset	N/A
HW Reset	N/A

**Flow Chart****9.52 Set Analog Control – ANCTLSET (0xE0)**

Please refer to relevant Application Note

## Revision Control

Revision	Date/Author	Remarks
2a	August 2010 / G Callow	First Preliminary issue
2b	October 2010 / G Callow	Alter top-level device description to OLED Driver

## Ordering Information

Datasheet

Title	DA8620-DS2b
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Product

Product Name	DA8620 240 x 320 OLED Driver
Package	
Shipment Form	Trays
Pack Quantity	
Order Code	DA8620-00-WD2-WO6

## Data Sheet Status Definitions

The Data Sheet version consists of two characters, a numeral followed by a lower-case alphabetic character. The numeral indicates Product Status (see table below), and the alphabetic character indicates the document revision level.

Version	Data Sheet Status	Product Status	Definition
1a – 1z	Draft	Development	Version 1 Data Sheets contain pre-tapeout information from the objective design specification. Dialog reserves the right to change the specification in any manner without notice
2a – 2z	Preliminary	Qualification	Version 2 data sheets contain information on post-tapeout and pre-volume production products. Dialog reserves the right to change the specification in any manner without notice, in order to supply the best possible product by improvements to the design. Relevant changes will be communicated via Dialog's Sales and Marketing departments
3a – 3z	Released	Production	Version 3 Data Sheets contain information on volume production products. Dialog reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notification

### Notes:

1. To avoid confusion, the following alphabetic characters shall not be used in document version references: **i, j, l, o**.
2. Please consult the latest issued version of the data sheet before initiating or completing a design.
3. The product status of the device may have changed since this data sheet was published.  
Please contact Dialog for the latest information.

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