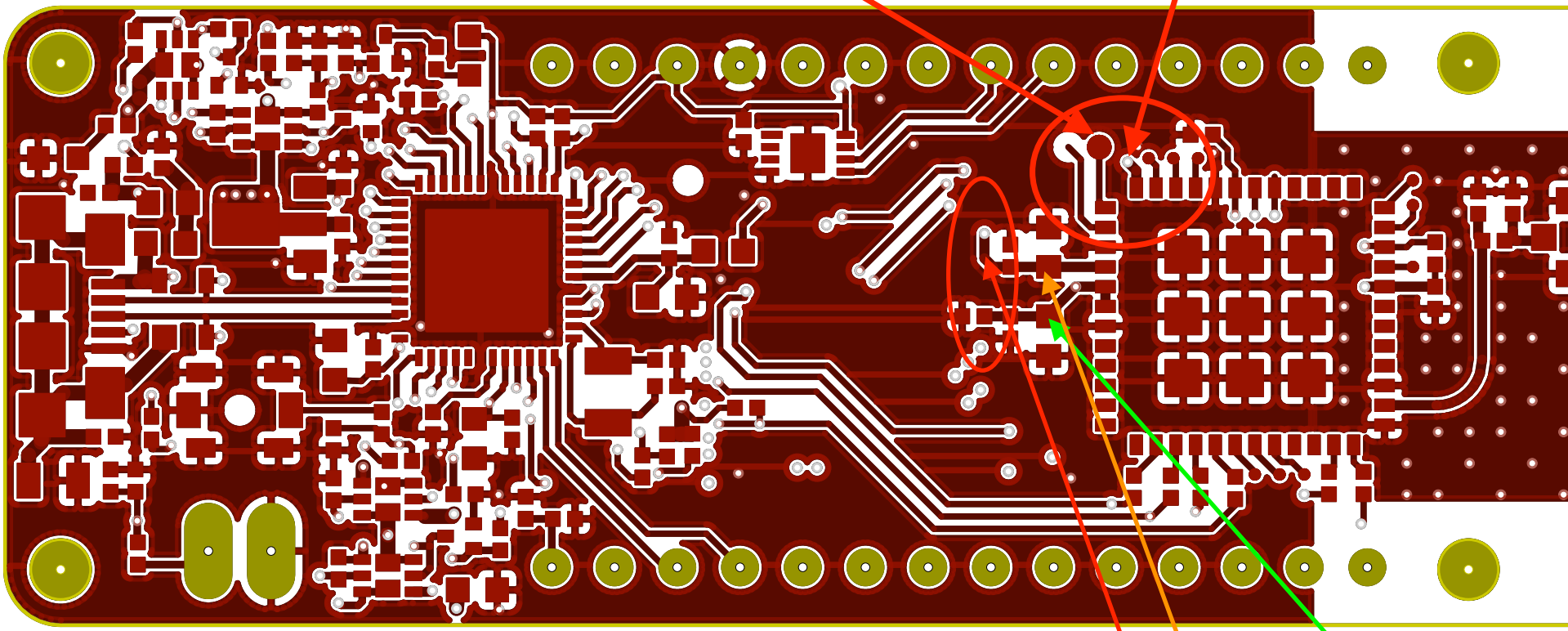
The via connecting pin 48 to the power plane must be disconnected from the power plane and pin 48 must connected to pin 1 via the test point connected to pin 1.

TOP LAYER

Option 1:

a) Drill this via to disconnect pin 48 from the power plane
b) Connect remaining copper trace to pin 1 test point on top layer

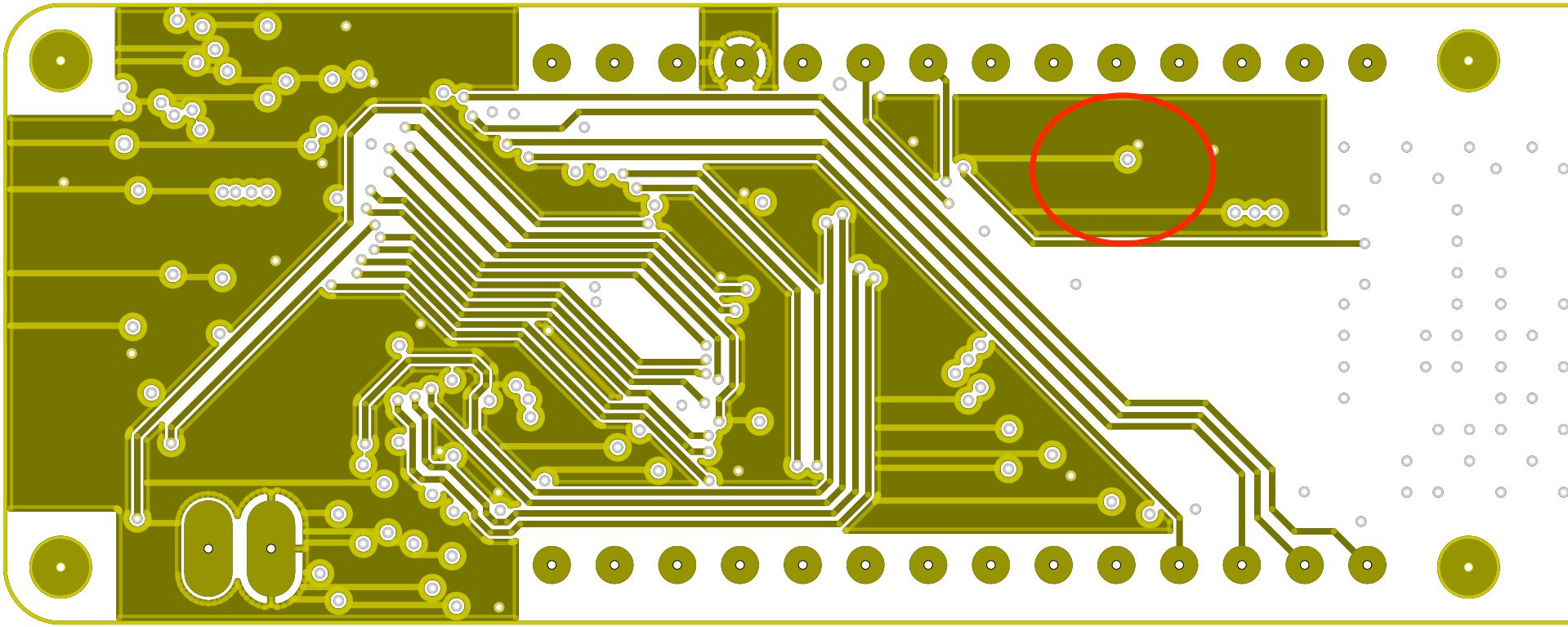
Pin1 test point



VDD_USB on pin 4 must be connected to VDD_MCU on pin 5.

a) Cut the +5V net before the via.
b) Connect the VDD_USB net to the 3.3V net

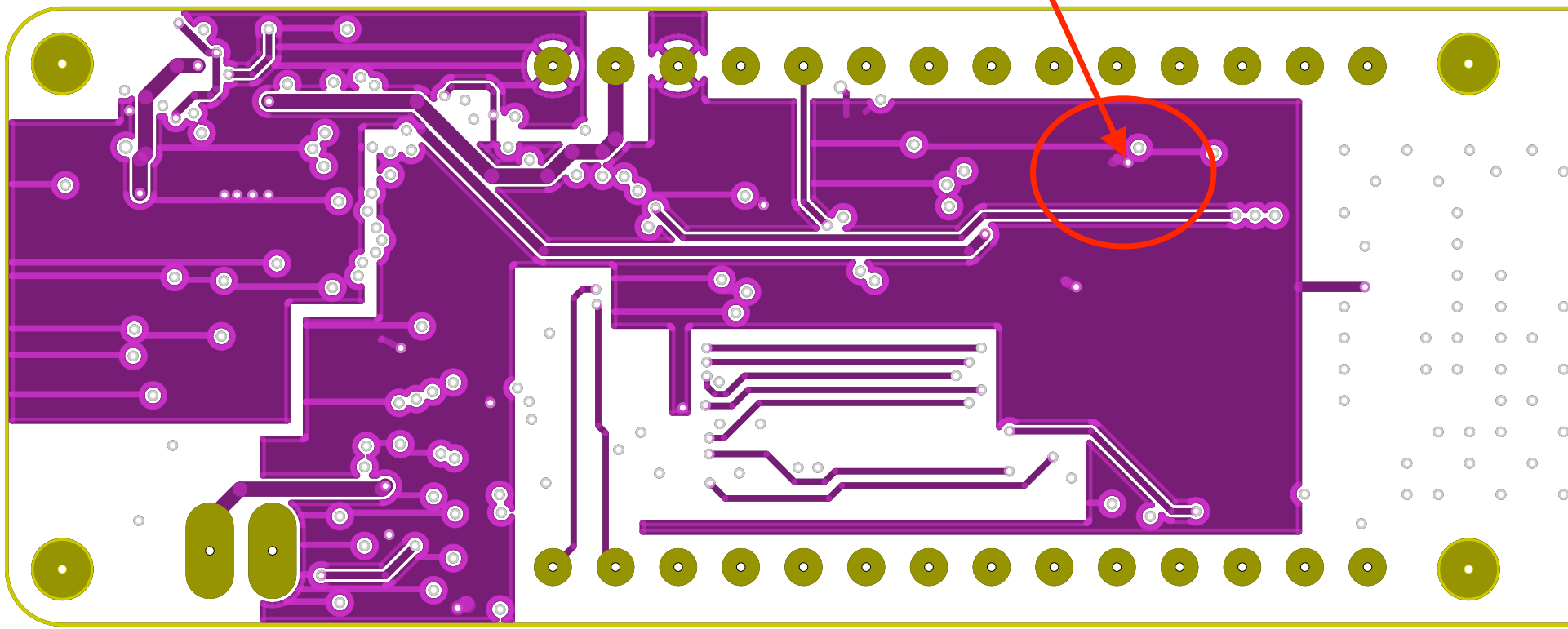
INNER LAYER 1



INNER LAYER 2

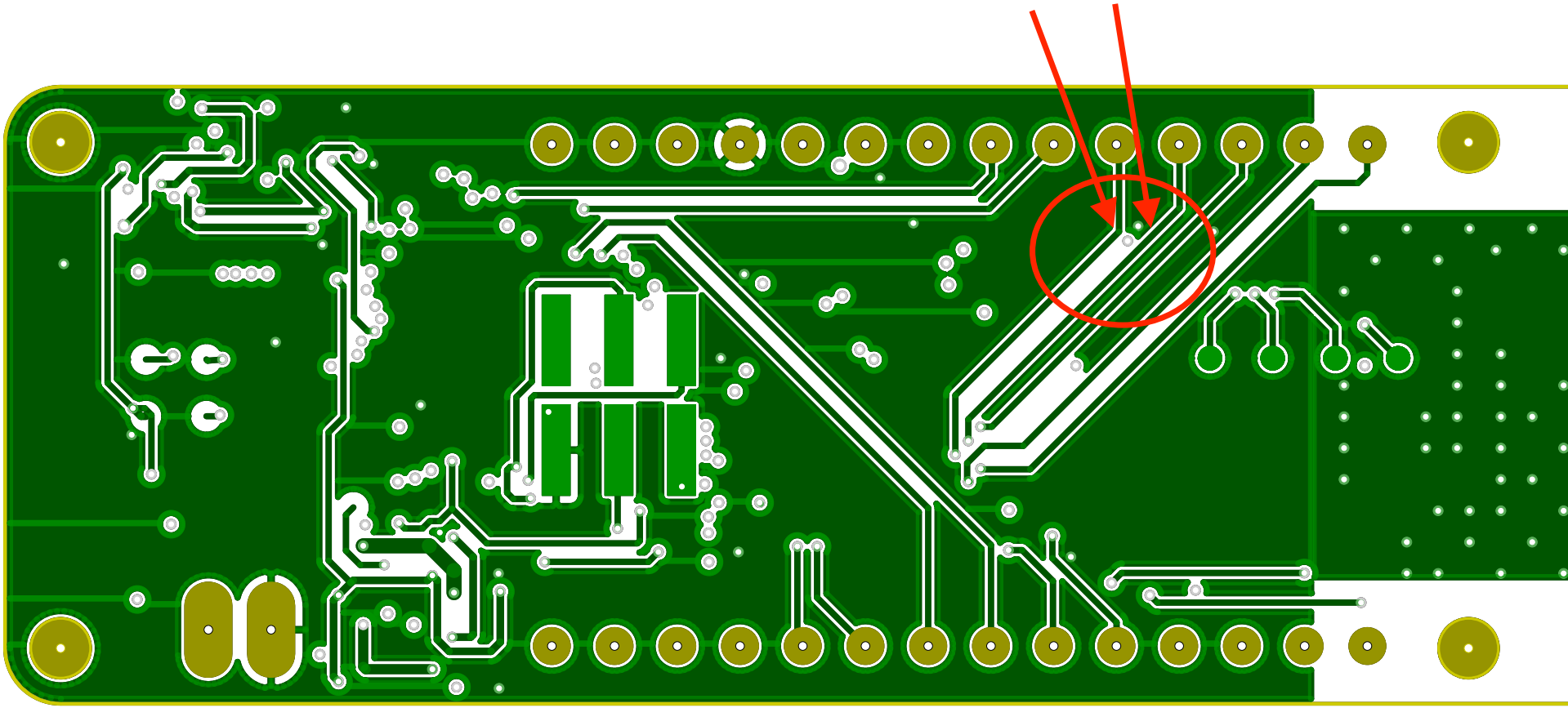
Option 2:

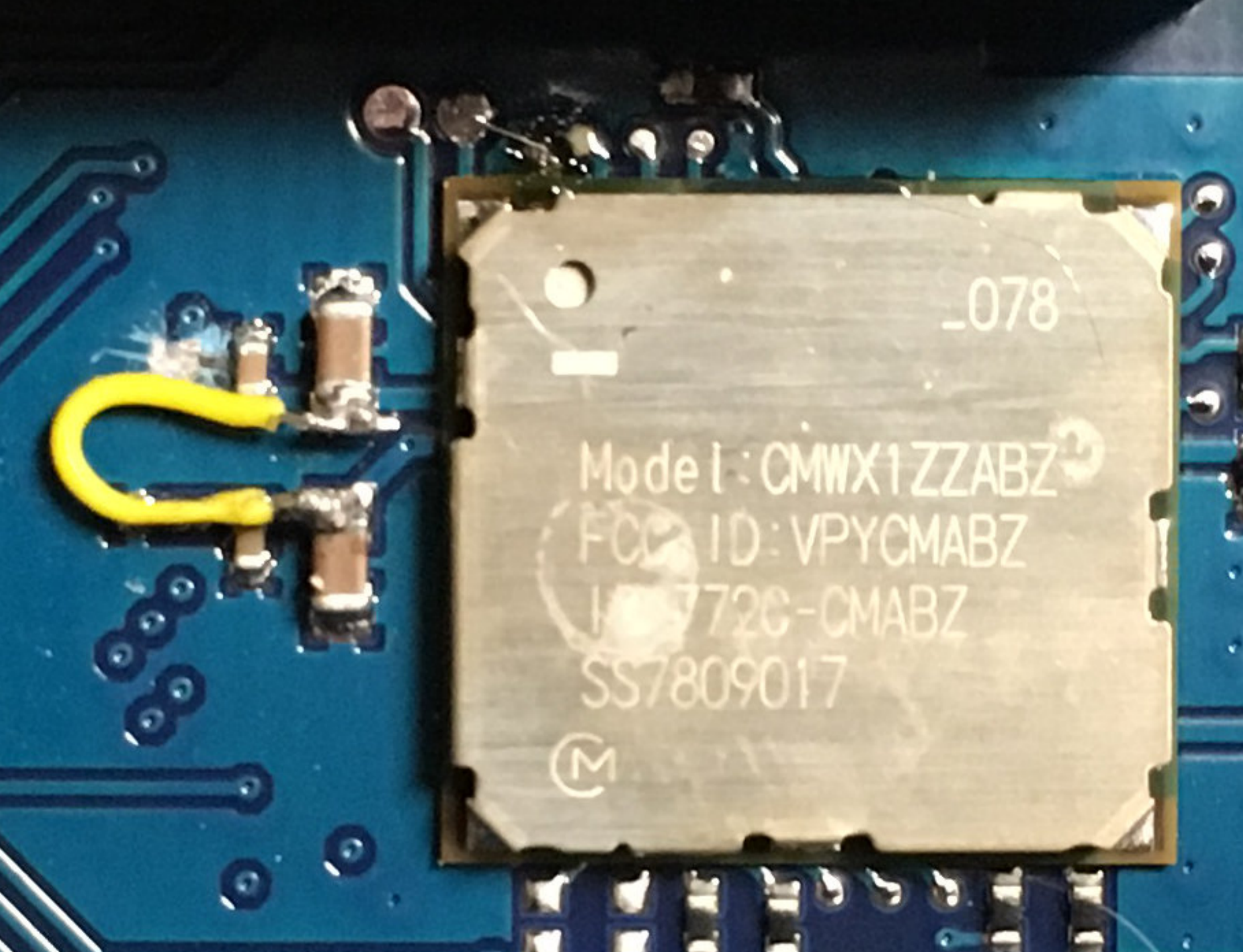
a) Laser cut an annulus around the via to disconnect from power plane.
b) Cut from the bottom layer and avoid cutting through the top layer.
c) Connect via to pin 1 test point on top layer.



BOTTOM LAYER

When laser cutting from the bottom, avoid cutting the adjacent signal traces

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SS7809017